

Features

- QSFP28 MSA compliant
- Compliant to IEEE 802.3bm 100GBASE PSM4
- Four independent full-duplex channels
- Supports 103.1Gb/s aggregate bit rate
- Up to 2km reach for G.652 SMF
- 4x25G electrical interface (OIF CEI-28G-VSR)
- Maximum power consumption 3.5W
- Single +3.3V power supply
- Operating case temperature: 0 to 70°C
- RoHS-6 compliant

Applications

- 100G Ethernet links
- Infiniband QDR and DDR interconnects
- Datacenter and Enterprise networking

Absolute Maximum Ratings

Parameter Parame	Symbol	Min.	Max.	Units	Note
Storage Temperature	Ts	-40	85	°C	
Operating Case Temperature	T_{op}	0	70	°C	
Supply Voltage	V_{cc}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH_d	3.0		dBm	

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Recommended Operating Conditions

Parameter Parameter	Symbol	Min.	Тур.	Max.	Units
Operating Case Temperature	T _{op}	0		70	$^{\circ}\!\mathbb{C}$
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Data Rate, each Lane			25.78125		Gb/s
Data Rate Accuracy		-100		100	ppm
Control Input Voltage High		2	A STATE OF THE PARTY OF THE PAR	Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance with G.652	D	0.002		2	km

Diagnostics Monitoring

Parameter	Symbol	Accuracy	Unit	Notes
Temperature monitor absolute error	DMI_Temp	± 3	°C	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	± 0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	± 2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	± 10%	mΑ	
Channel TX power monitor absolute error	DMI_TX_Ch	± 2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

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Transmitter Electro-optical Characteristics (each Lane)

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				3.5	W	· ·
Supply Current	lcc			1.06	Α	
Overload Differential Voltage pk-pk	TP1a	900			mV	
Common Mode Voltage (Vcm)	TP1	-350		2850	mV	1
Differential Termination Resistance Mismatch	TP1			10	%	At 1MHz
Differential Return Loss (SDD11)	TP1			See CEI- 28G- VSR Equation 13-19	dB	
Common Mode to Differential conversion and		~	Mr	See CEI- 28G-		
Differential to Common Mode conversion	TP1			VSR Equation	dB	
(SDC11, SCD11)				13-20		
Stressed Input Test	TP1a	See CEI- 28G-VSR Section 13.3.11.2.1				
Center Wavelength	λс	1295	1310	1325	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	PT	7		8	dBm	
Average Launch Power, each Lane	Pavg	-5.5		2	dBm	
Optical Modulation Amplitude (OMA), each Lane	Рома	-3.5		2.2	dBm	2
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-4.3			dBm	
TDP, each Lane	TDP			2.9	dB	
Extinction Ratio	ER	3.5			dB	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R⊤			-12	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Transmitter Eye Mask Definition {0.31, 0.4, 0.45, 0.34, 0.38, 0.4} {X1, X2, X3, Y1, Y2, Y3}						

Notes:

- 1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
- 2. 1. Even if the TDP < 0.8 dB, the OMA min must exceed the minimum value specified here.

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Receiver Electro-optical Characteristics (each Lane)

Parameter	Test Point	Min	Typical	Max	Units	Notes
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (Vcm)	TP4	-350		2850	mV	1
Common Mode Noise, RMS	TP4			17.5	mV	
Differential Termination Resistance Mismatch	TP4			10	%	At 1MHz
Differential Return Loss (SDD22)	TP4	4		See CEI- 28G- VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)	TP4	4	ک	See CEI- 28G- VSR Equation 13-21	dB	
Common Mode Return Loss (SCC22)	TP4		1	-2	dB	2
Transition Time, 20 to 80%	TP4	9.5	> /		ps	
Vertical Eye Closure (VEC)	TP4	1-	-	5.5	dB	
Eye Width at 10 ⁻¹⁵ probability (EW15)	TP4	0.57			UI	
Eye Height at 10 ⁻¹⁵ probability (EH15)	TP4	228	11		mV	
Center Wavelength	λс	1295	1310	1325	nm	
Damage Threshold, each Lane	TH₀	3	_		dBm	3
Average Receive Power, each Lane		-10.2		2	dBm	
Receive Power (OMA), each Lane				2.2	dBm	
Receiver Sensitivity (OMA), each Lane	SEN1			-9	dBm	for BER = 1x10 ⁻¹²
Stressed Receiver Sensitivity (OMA), each Lane				-6.44	dBm	for BER = $1x10^{-12}$
Receiver Sensitivity (OMA), each Lane	SEN2			-11.35	dBm	for BER = 5x10 ⁻⁵
Stressed Receiver Sensitivity (OMA), each Lane				-8.79	dBm	for BER = 5x10 ⁻⁵
Receiver Reflectance	R _R			-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			31	GHz	

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Conditions of Stress Receiver Sensitivity Test (Note 4)						
Vertical Eye Closure Penalty, each Lane	1.9	dB				
Stressed Eye J2 Jitter, each Lane	0.27	UI				
Stressed Eye J4 Jitter, each Lane	0.39	UI				
Stressed Eye Mask Definition						
{X1, X2, X3, Y1, Y2, Y3}	{0.24, 0.5, 0.5, 0.24, 0.24, 0.4}					

Notes:

- 1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
- 2. From 250MHz to 30GHz.
- 3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
- 4. Vertical eye closure penalty, stressed eye J2 jitter, stressed eye J4 jitter, and stressed receiver eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

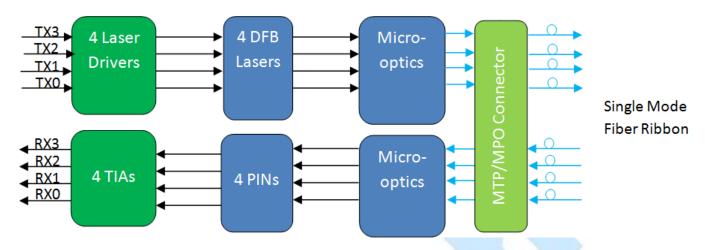
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Block Diagram of Transceiver



This product is a parallel 100Gb/s Quad Small Form-factor Pluggable (QSFP28) optical module. It provides increased port density and total system cost savings. The QSFP28 full- duplex optical module offers 4 independent transmit and receive channels, each capable of 25Gb/s operation for an aggregate data rate of 100Gb/s on 2km of single mode fiber.

An optical fiber ribbon cable with an MTP/MPO connector can be plugged into the QSFP28 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an MSA-compliant 38-pin edge type connector.

The module operates with single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module can be managed through the I2C two-wire serial interface.

This product is a QSFP28 parallel single mode optical transceiver with an MTP/MPO fiber ribbon connector. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 25Gb/s per channel. Figure 1 shows the functional block diagram of this product.

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A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. Per MSA the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL. Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP28 module must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.

The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

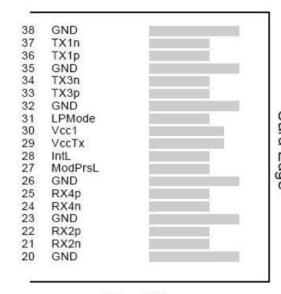
Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a "Low" state.

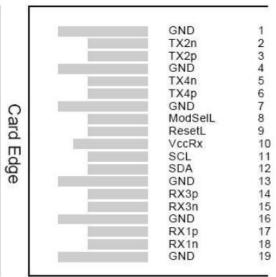
Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

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Pin Assignment





Top Side Viewed from Top

Bottom Side Viewed from Bottom

MSA compliant Connector

Pin Description

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSeIL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GNC	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data output	
15	CML-O	Rx3n	Receiver Inverted Data output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	

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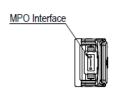
18 CML-O Rx1n Receiver Inverted Data Output 19 GND Ground 20 GND Ground 21 CML-O Rx2n Receiver Inverted Data output 22 CML-O Rx2p Receiver Non-Inverted Data output 23 GND Ground 24 CML-O Rx4n Receiver Inverted Data output 25 CML-O Rx4p Receiver Non-Inverted Data output 26 GND Ground 27 LVTTL-O ModPrsL Module Present 28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Input 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input 37 CML-I Tx1n Transmitter Inverted Data Output	PIN	Logic	Symbol	Name/Description	Note
20 GND Ground 21 CML-O Rx2n Receiver Inverted Data output 22 CML-O Rx2p Receiver Non-Inverted Data output 23 GND Ground 24 CML-O Rx4n Receiver Inverted Data output 25 CML-O Rx4p Receiver Non-Inverted Data output 26 GND Ground 27 LVTTL-O ModPrsL Module Present 28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	18	CML-O	Rx1n	Receiver Inverted Data Output	
21 CML-O Rx2n Receiver Inverted Data output 22 CML-O Rx2p Receiver Non-Inverted Data output 23 GND Ground 24 CML-O Rx4n Receiver Inverted Data output 25 CML-O Rx4p Receiver Non-Inverted Data output 26 GND Ground 27 LVTTL-O ModPrsL Module Present 28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	19		GND	Ground	1
22 CML-O Rx2p Receiver Non-Inverted Data output 23 GND Ground 24 CML-O Rx4n Receiver Inverted Data output 25 CML-O Rx4p Receiver Non-Inverted Data output 26 GND Ground 27 LVTTL-O ModPrsL Module Present 28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	20		GND	Ground	1
GND Ground CML-O Rx4n Receiver Inverted Data output CML-O Rx4p Receiver Non-Inverted Data output GND Ground CML-O ModPrsL Module Present Receiver Non-Inverted Data output CML-O ModPrsL Module Present Interrupt VccTx +3.3V Power Supply transmitter Vcc1 +3.3V Power Supply LVTTL-I LPMode Low Power Mode GND Ground CML-I Tx3p Transmitter Non-Inverted Data Input CML-I Tx3n Transmitter Inverted Data Output GND Ground CML-I Tx3n Transmitter Inverted Data Output GND Ground GND Ground Tx1p Transmitter Non-Inverted Data Input	21	CML-O	Rx2n	Receiver Inverted Data output	
24 CML-O Rx4n Receiver Inverted Data output 25 CML-O Rx4p Receiver Non-Inverted Data output 26 GND Ground 27 LVTTL-O ModPrsL Module Present 28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	22	CML-O	Rx2p	Receiver Non-Inverted Data output	
25 CML-O Rx4p Receiver Non-Inverted Data output 26 GND Ground 27 LVTTL-O ModPrsL Module Present 28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	23		GND	Ground	1
GND Ground 27 LVTTL-O ModPrsL Module Present 28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	24	CML-O	Rx4n	Receiver Inverted Data output	1
27 LVTTL-O ModPrsL Module Present 28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	25	CML-O	Rx4p	Receiver Non-Inverted Data output	
28 LVTTL-O IntL Interrupt 29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	26		GND	Ground	1
29 VccTx +3.3V Power Supply transmitter 30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	27	LVTTL-O	ModPrsL	Module Present	
30 Vcc1 +3.3V Power Supply 31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	28	LVTTL-O	IntL	Interrupt	
31 LVTTL-I LPMode Low Power Mode 32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	29		VccTx	+3.3V Power Supply transmitter	2
32 GND Ground 33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	30		Vcc1	+3.3V Power Supply	2
33 CML-I Tx3p Transmitter Non-Inverted Data Input 34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	31	LVTTL-I	LPMode	Low Power Mode	
34 CML-I Tx3n Transmitter Inverted Data Output 35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	32		GND	Ground	1
35 GND Ground 36 CML-I Tx1p Transmitter Non-Inverted Data Input	33	CML-I	Тх3р	Transmitter Non-Inverted Data Input	
36 CML-I Tx1p Transmitter Non-Inverted Data Input	34	CML-I	Tx3n	Transmitter Inverted Data Output	
	35		GND	Ground	1
37 CML-I Tx1n Transmitter Inverted Data Output	36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
	37	CML-I	Tx1n	Transmitter Inverted Data Output	
38 GND Ground	38		GND	Ground	1

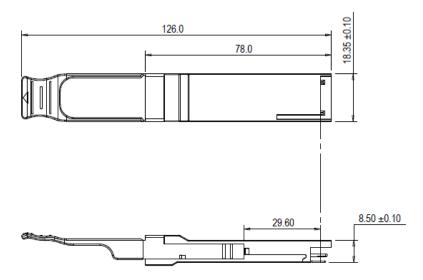
Notes:

- 1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
- 2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and VccTx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

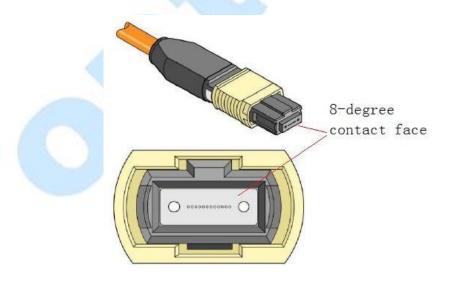
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Dimensions





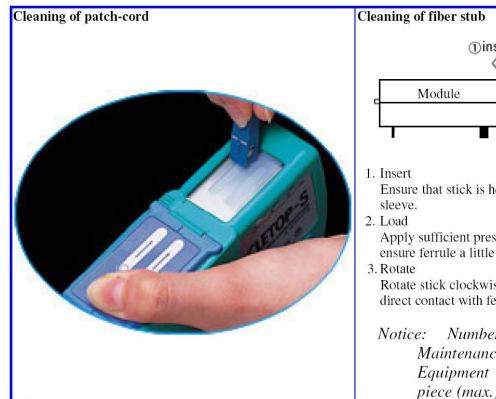
Attention: To minimize MPO connection induced reflections, an MPO receptacle with 8- degree angled end-face is utilized for this product. A female MPO connector with 8-degree end-face should be used with this product as illustrated in below figure.

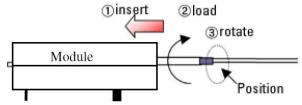


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Optical Receptacle Cleaning Recommendations:

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.





- Ensure that stick is held straight when inserting into
- Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve.
- Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained.

Number of possible *Maintenance* (repair) ~1 use / piece Equipment construction: 4 uses piece (max.)

Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

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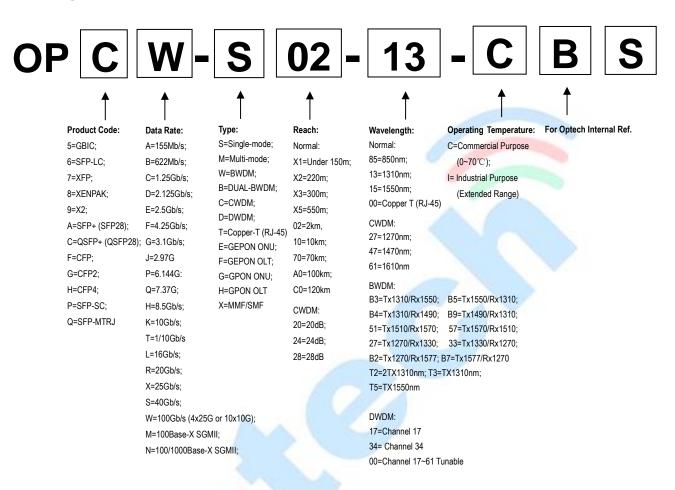
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Ordering Information



Model Number	Part Number	Voltage	Temperature
QSFP28-IR4-PSM	OPCW-S02-13-CBS	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.

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