

Features

- QSFP28 MSA compliant
- 4 CWDM lanes MUX/DEMUX design
- Supports 103.1Gb/s aggregate bit rate
- Compliant to 100G CWDM4 MSA Technical Spec Rev1.1
- Bidirectional optical data transmission/receiving
- Up to 2km transmission on single mode fiber (SMF) with FEC
- Operating case temperature: 0 to 70°C
- 4x25G electrical interface (OIF CEI-28G-VSR)
- Maximum power consumption 3.5W
- Optical connector: SMF angled polished LC simplex connector
- Hot pluggable: the module needs to be hot pluggable for ease of installation and service
- RoHS compliant

Applications

- Data Center Interconnect
- 100G Ethernet
- 100G Campus Link

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T _s	-40	85	°C	
Operating Case Temperature	T _{op}	0	70	°C	
Supply Voltage	V _{cc}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH _d	3.5		dBm	

Recommended Operating Conditions and Power Supply Requirement

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Case Temperature	T _{op}	0		70	°C
Power Supply Voltage	V _{cc}	3.135	3.3	3.465	V
Data Rate, each Lane			25.78125		Gb/s
Data Rate Accuracy		-100		100	ppm
Control Input Voltage High		2		V _{cc}	V
Control Input Voltage Low		0		0.8	V
Link Distance with G.652	D	0.002		10	km

Diagnostics Monitoring

Parameter	Symbol	Accuracy	Unit	Notes
Temperature monitor absolute error	DMI_Temp	± 3	°C	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	± 0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	± 2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	± 10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	± 2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Transmitter Electro-optical Characteristics (each Lane)

Parameter	Test Point	Min	Typ.	Max	Units	Notes
Power Consumption				3.5	W	
Supply Current	I _{cc}			1.06	A	
Overload Differential Voltage pk-pk	TP1a	900			mV	
Common Mode Voltage (V _{cm})	TP1	-350		2850	mV	1
Differential Termination Resistance Mismatch	TP1			10	%	At 1MHz
Differential Return Loss (SDD11)	TP1			See CEI-28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)	TP1			See CEI-28G-VSR Equation 13-20	dB	
Stressed Input Test	TP1a		See CEI-28G-VSR Section 13.3.11.2.1			
Lane Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P _T			8.5	dBm	
Average Launch Power, each Lane	P _{AVG}	-6.5		2.5	dBm	
Optical Modulation Amplitude (OMA), each Lane	P _{OMA}	-4		2.5	dBm	2
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-5			dBm	
TDP, each Lane	TDP			3.0	dB	
Extinction Ratio	ER	3.5			dB	

<i>Parameter</i>	<i>Test Point</i>	<i>Min</i>	<i>Typ.</i>	<i>Max</i>	<i>Units</i>	<i>Notes</i>
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R _T			-12	dB	
Average Launch Power OFF Transmitter, each Lane	P _{off}			-30	dBm	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}				{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}		3

Notes:

1. V_{cm} is generated by the host. Specification includes effects of ground offset voltage.
2. Even if the TDP < 1.0 dB, the OMA min must exceed the minimum value specified here.
3. Hit ratio 5x10⁻⁵.



Receiver Electro-optical Characteristics (each Lane)

<i>Parameter</i>	<i>Test Point</i>	<i>Min</i>	<i>Typ.</i>	<i>Max</i>	<i>Units</i>	<i>Notes</i>
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (Vcm)	TP4	-350		2850	mV	1
Common Mode Noise, RMS	TP4			17.5	mV	
Differential Termination Resistance Mismatch	TP4			10	%	At 1MHz
Differential Return Loss (SDD22)	TP4			See CEI-28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)	TP4			See CEI-28G-VSR Equation 13-21	dB	
Common Mode Return Loss (SCC22)	TP4			-2	dB	2
Transition Time, 20 to 80%	TP4	9.5			ps	
Vertical Eye Closure (VEC)	TP4			5.5	dB	
Eye Width at 10 ⁻¹⁵ probability (EW15)	TP4	0.57			UI	
Eye Height at 10 ⁻¹⁵ probability (EH15)	TP4	228			mV	
Damage Threshold, each Lane	TH _d	3.5			dBm	3
Average Receive Power, each Lane		-11.5		2.5	dBm	
Receive Power (OMA), each Lane				2.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-10	dBm	For BER = 5x10 ⁻⁵
Stressed Receiver Sensitivity (OMA), each Lane				-7.3	dBm	4
Receiver Reflectance	R _R			-26	dB	
LOS Assert	LOSA	-30			dBm	

Parameter	Test Point	Min	Typ.	Max	Units	Notes
LOS Deassert	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3dB upper Cutoff Frequency, each Lane	Fc			31	GHz	

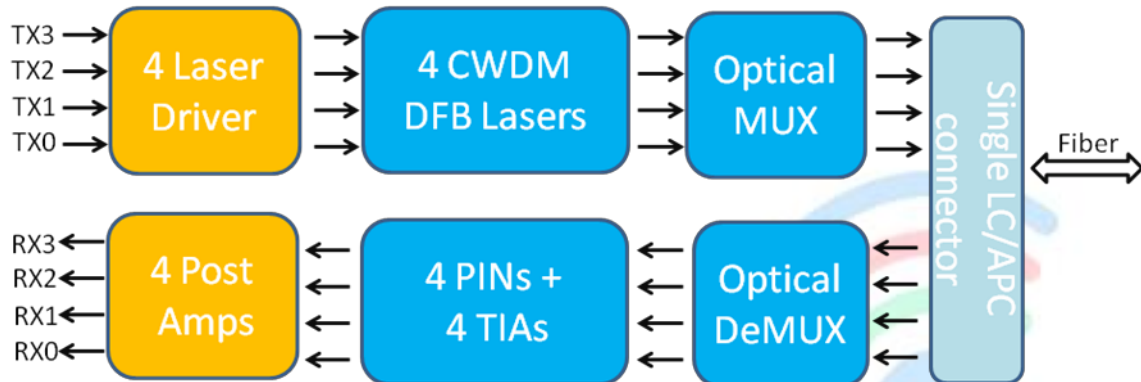
Conditions of Stress Receiver Sensitivity Test (Note 5)

Vertical Eye Closure Penalty, each Lane			1.9		dB	
Stressed Eye J2 Jitter, each Lane			0.33		UI	
Stressed Eye J4 Jitter, each Lane			0.48		UI	
SRS eye mask definition { X1, X2, X3, Y1, Y2, Y3}						{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}

Notes:

1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. From 250MHz to 30GHz.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal for BER = 5×10^{-5} .
5. Vertical eye closure penalty, stressed eye J2 jitter, stressed eye J4 jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Block Diagram of Transceiver



This product converts the 4-channel 25Gb/s electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 100Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 100Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 25Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified by a TIA and a post amplifier. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

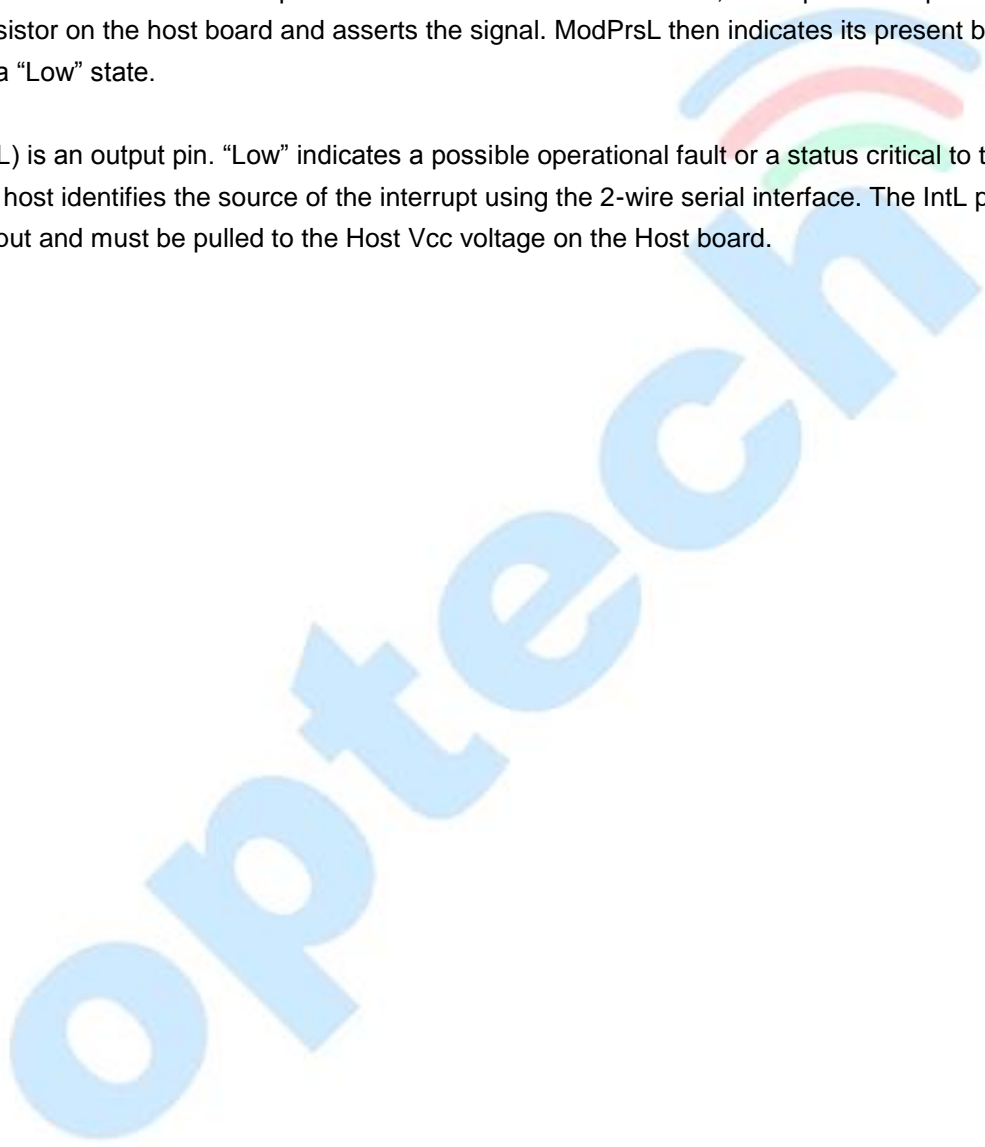
Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

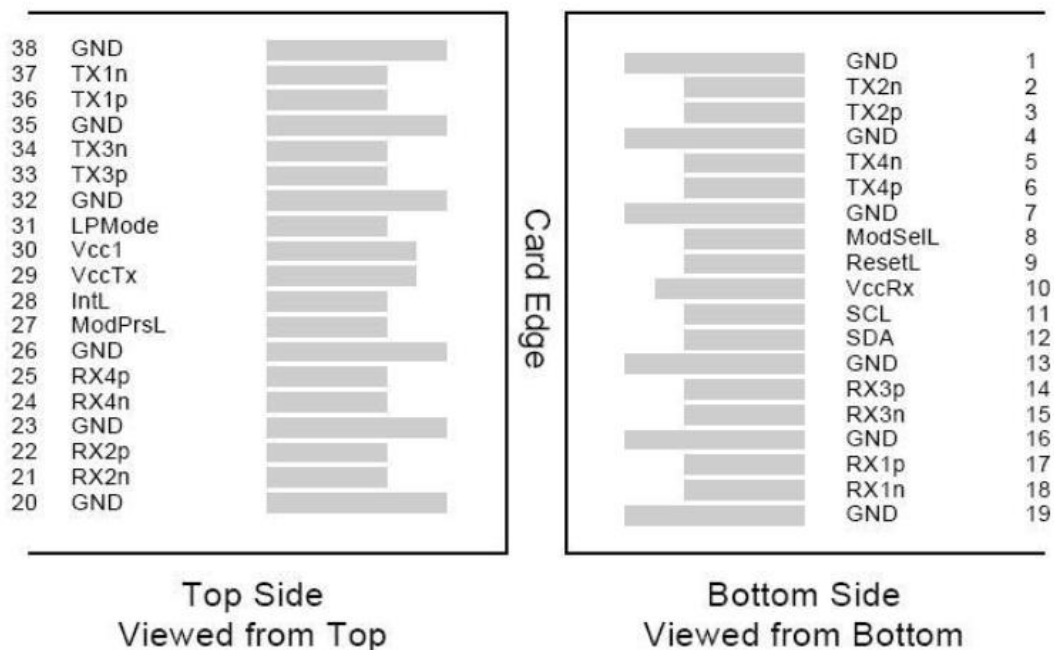
Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.



Pin Assignment



MSA compliant Connector

Pin Description

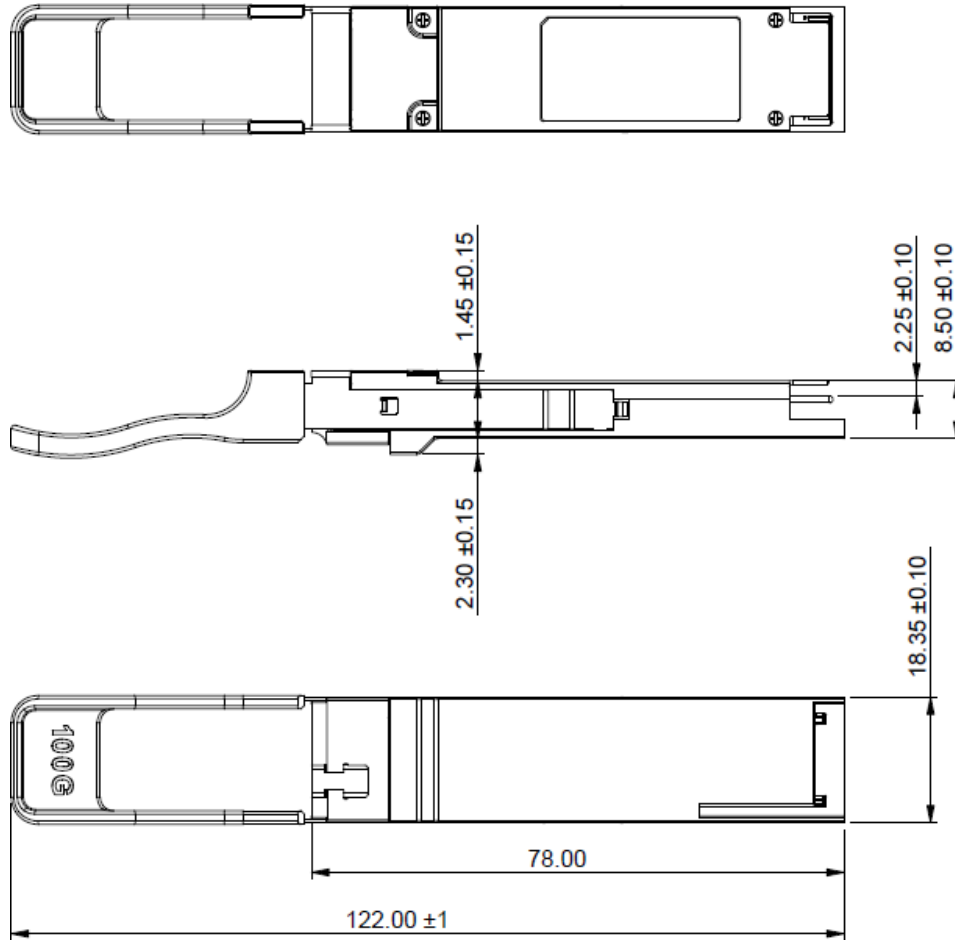
PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data output	
15	CML-O	Rx3n	Receiver Inverted Data output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	

PIN	Logic	Symbol	Name/Description	Note
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data output	
22	CML-O	Rx2p	Receiver Non-Inverted Data output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Note:

- GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
- VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.


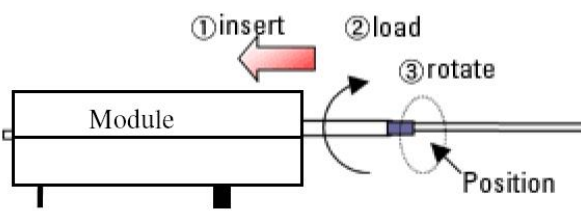
Dimensions



Optical Receptacle Cleaning Recommendations :

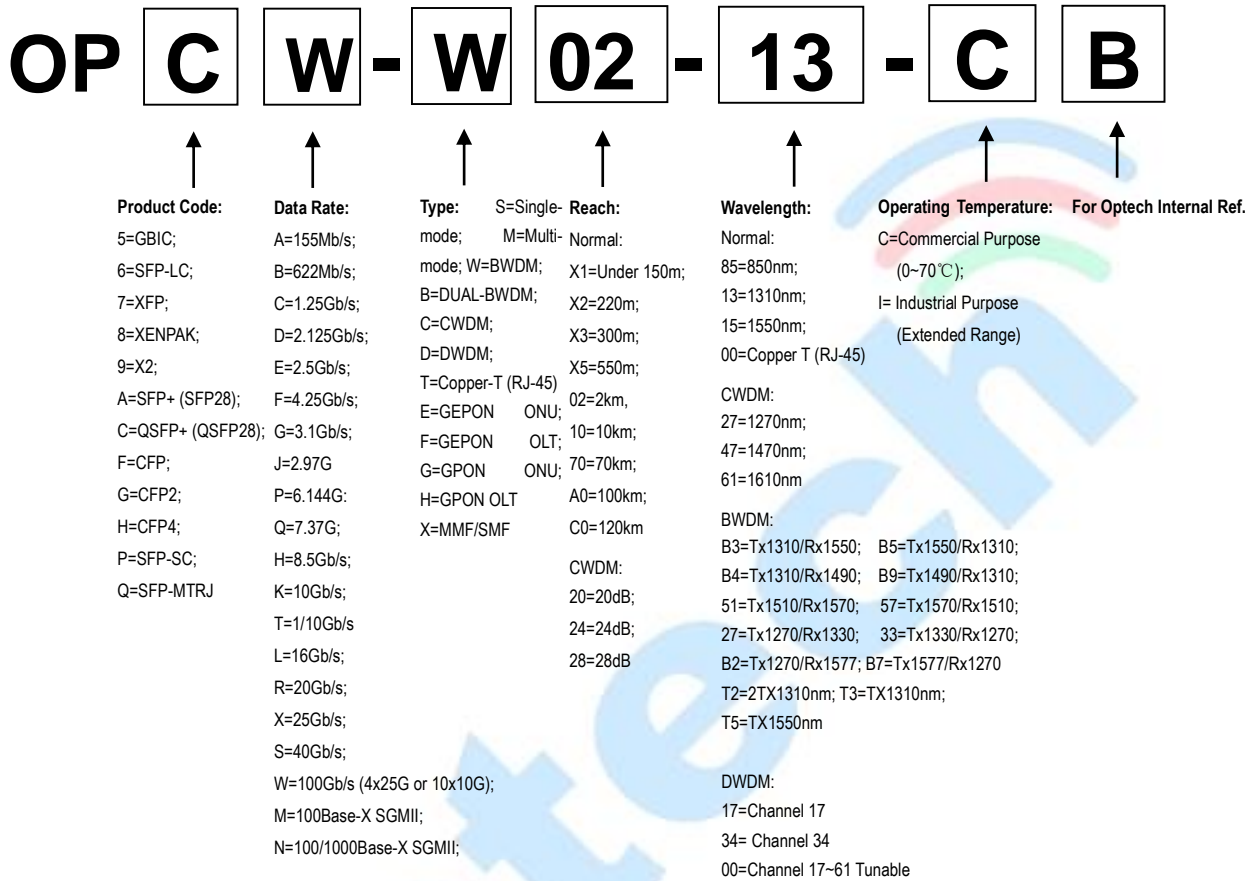
All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.



<p>Cleaning of patch-cord</p> 	<p>Cleaning of fiber stub</p>  <ol style="list-style-type: none"> 1. Insert Ensure that stick is held straight when inserting into sleeve. 2. Load Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve. 3. Rotate Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained. <p><i>Notice: Number of possible wipes: Maintenance (repair) ~1 use / piece Equipment construction: 4 uses / piece (max.)</i></p>
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Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information



Model Number	Part Number	Voltage	Temperature
QSFP28-100G-BWDM-CWDM4	OPCW-W02-13-CB	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.