Features

- QSFP-DD MSA compliant
- 8 parallel full-duplex channels
- Compliant to IEEE802.3bs
- Up to 100m OM3 MMF transmission
- Operating case temperature: 0 to 70ºC
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 53.125Gbps (PAM4) per channel.
- Maximum power consumption 12W
- RoHS compliant

Applications

- 400G Ethernet
- Infiniband EDR

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	Ts	–40	85	°C	
Operating Case Temperature	T_{OP}	0	70	°C	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Units	Note
Operating Case Temperature	T_{OP}	0		70	°C	
Power Supply Voltage	*Vcc*	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		Gbd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance with OM3	*D*	0.5		100	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics – Transmitter

Parameter	Test point	Min.	Typical	Max.	Units	Note
Power Consumption				12	W	
Supply Current	*Icc*			3.63	A	
Signaling Rate, each Lane	*TP1*		26.5625 ± 100ppm		GBd	
Differential pk-pk Input Voltage Tolerance	*TP1a*	900			mVpp	1
Differential Termination Mismatch	*TP1*			10	%	
Differential Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	*TP1a*	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	*TP1a*		-0.4 to 3.3		V	
DC Common Mode Input Voltage	*TP1*	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

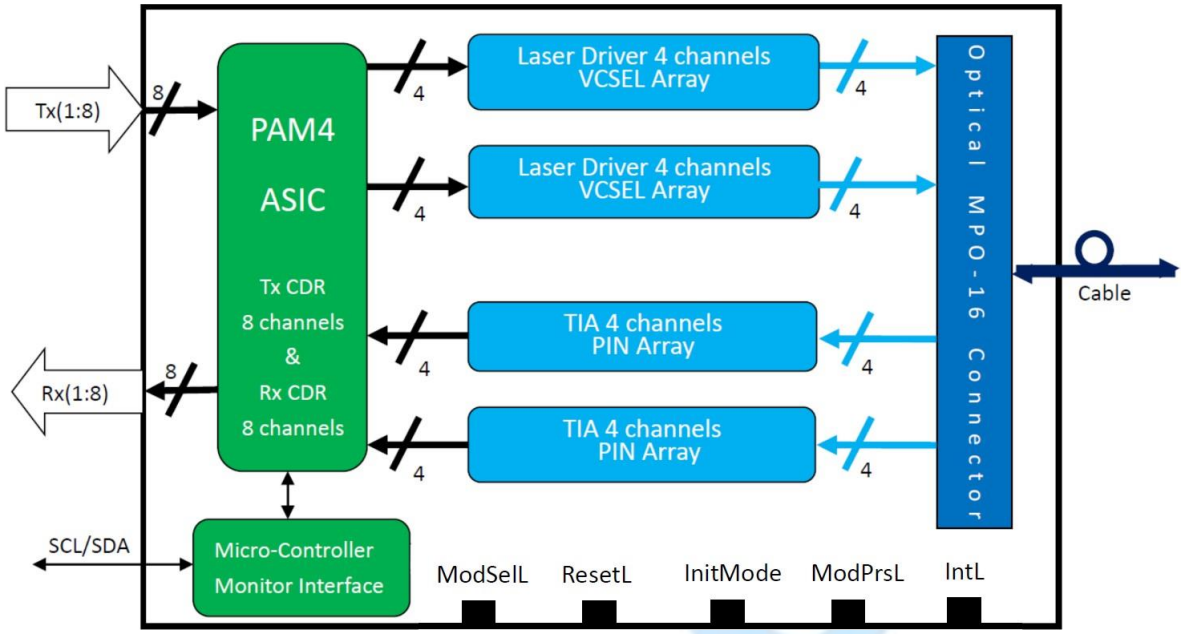
Electrical Characteristics – Receiver

Parameter	Test point	Min.	Typical	Max.	Units	Note
Signaling Rate, each Lane	*TP4*		26.5625 ± 100ppm		GBd	
Differential pk-pk Output Voltage	*TP4*			900	mVpp	
AC Common Mode Output Voltage, RMS	*TP4*			17.5	mV	
Differential Termination Mismatch	*TP4*			10	%	
Differential Output Return Loss	*TP4*	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	*TP4*	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	*TP4*	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	*TP4*		0.265		UI	
Near-end Eye Height, Differential	*TP4*	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	*TP4*		0.2		UI	
Far-end Eye Height, Differential	*TP4*	30			mV	
Far-end Pre-cursor ISI Ratio	*TP4*	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	*TP4*	-350		2850	mV	1

Notes:

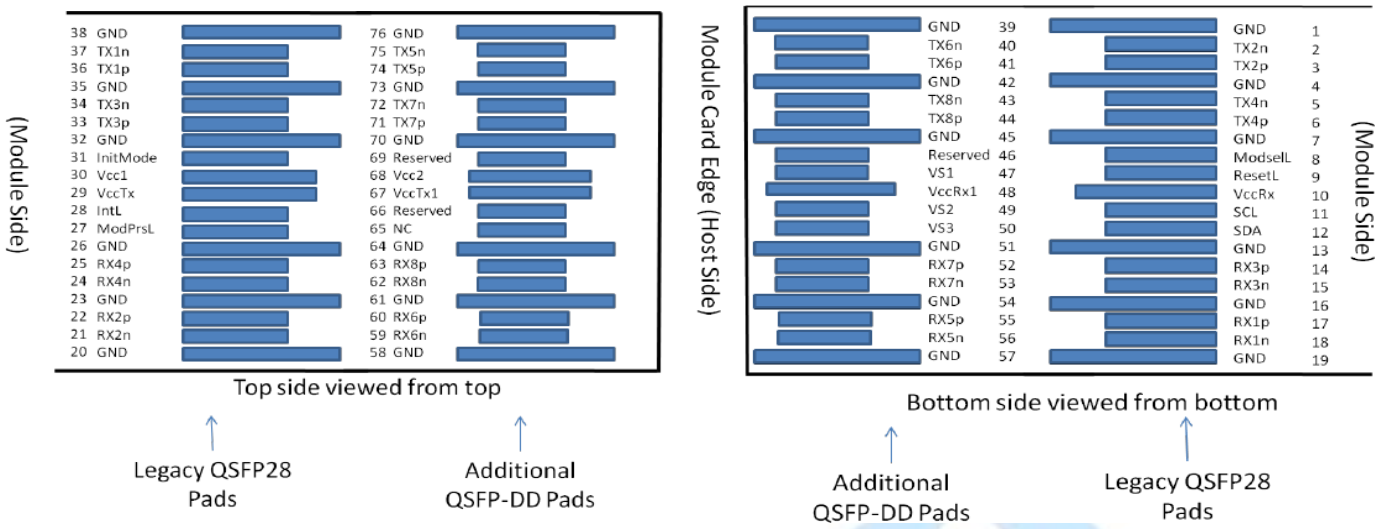
1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

AOC Block Diagram



Block Diagram of One of the QSFP-DD AOC End Modules

Pin Assignment



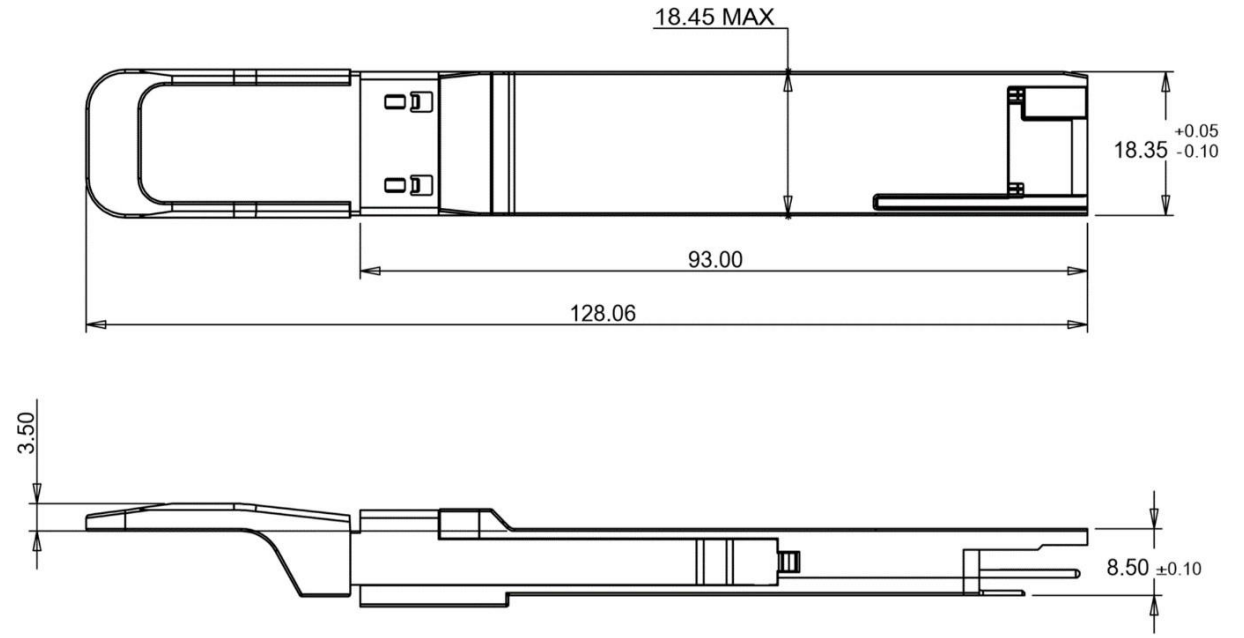
Pin Definition

Pin #	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B

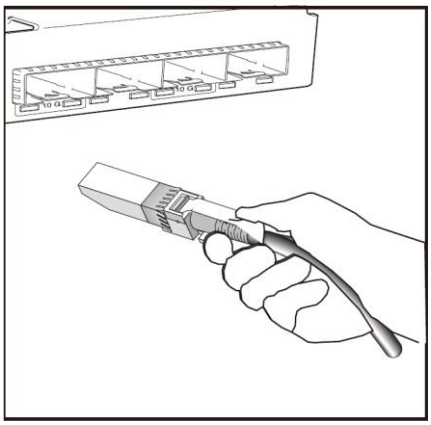
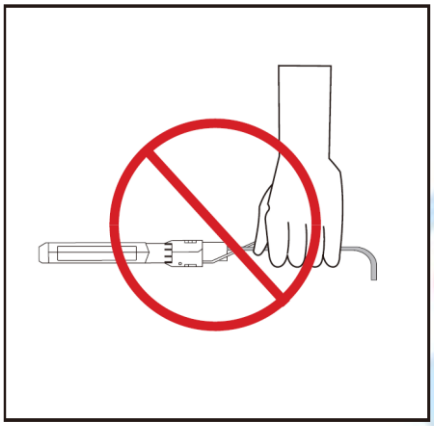
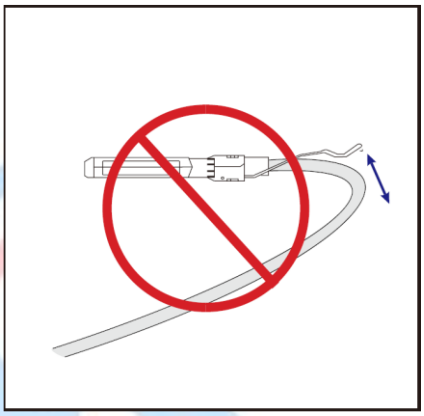
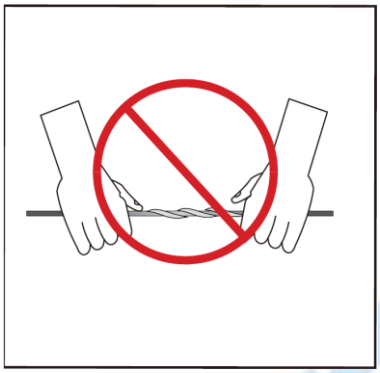
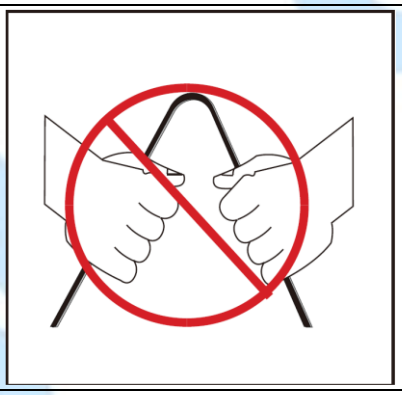
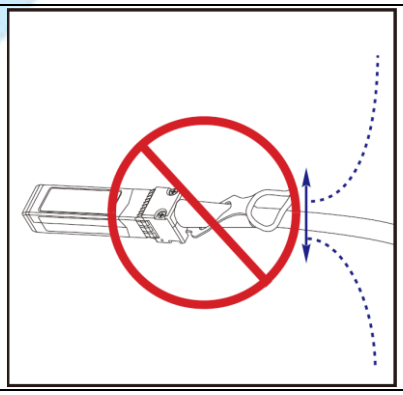
Pin #	Logic	Symbol	Description	Plug Sequence
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A

Pin #	Logic	Symbol	Description	Plug Sequence
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For Future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

Dimensions



Important Notice

		
Holding the SFP+ connector by its sides, insert the connector into the port on the switch	Do not handle by cable	DO NOT Over-bend the cable behind the connector
		
DO NOT twist the cable	DO NOT kink the cable	DO NOT bend up and down the cable

Ordering Information

OP [QSDD] - [F] - [01] - [A] [K] [T]

Product Code:
MSAS= Mini-SAS;
MSHD=Mini-SAS HD 6~12G;
SFPP=SFP+ 8~10G;
MSFP=Mini SFP;
XFP=XFP 10G;
CX4=CX4 10G;
QDDR=QDDR 20G;
SF28=SFP28 25G;
QSFP=QSFP 40G;
QFDR=FDR 56G;
QS28=QSFP28 100G;
CXP=CXP 120G
QSDD=QSFP-DD

Transceiver Type:
T=Electrical;
F=Optical;
I=Internal Electrical

Cable Length:
X5=0.5M;
01=1M;
03=3M;
05=5M;
07=7M;
10=10M;
15=15M;
20=20M;
A0=100M
xxxx=Customized Length (Unit: CM)
A5=1.5M (For 25G &100G only);
B5=2.5M (For 25G &100G only);
C5=3.5M (For 25G &100G only)
For Loopback Attenuation:
00=0dB;
0A=1dB;
0B=2dB;
0C=3dB;
0D=4dB;
0E=5dB

P=Passive;
A=Active;

DAC AWG:
A=24;
B=26;
C=28;
E=30;
F=32
X=No Media Type (For Loopback)
AOC OD:
K=3.0 mm
For Loopback Power Consumption:
X=0W;
1=1W;
A=1.5W;
2=2W;
B=2.5W;
3=3W;
C=3.5W
4=4W;
5=5W

For Optech Internal ref.

Part Number	Model Number	Length (M)	Voltage	Temperature
OPQSDD-F-03-AKT	Active Optical Cable	3	3.3V	0°C ~ 70°C
OPQSDD-F-05-AKT	Active Optical Cable	5	3.3V	0°C ~ 70°C
OPQSDD-F-07-AKT	Active Optical Cable	7	3.3V	0°C ~ 70°C

Note: All information contained in this document is subject to change without notice.