

Features

- QSFP56 MSA compliant
- 4 parallel lanes on 850nm center wavelength
- Compliant to IEEE 802.3cd Specification
- Up to 70m transmission on multi-mode fiber (MMF) OM3 with FEC
- Operating case temperature: 0 to 70°C
- 4x53.125Gb/s electrical interface (200GAUI-4)
- Data Rate 53.125Gbps (PAM4) per channel.
- Maximum power consumption 5W
- RoHS compliant



Applications

- Data Center Interconnect
- 200G Ethernet
- Infiniband interconnects
- Enterprise networking

Description

This product is a high data rate parallel active optical cable (AOC), to overcome the bandwidth limitation of traditional copper cable. The AOC offers 4 independent data transmission channels and 4 data receiving channels via a multimode fiber cable, each capable of 50Gb/s operation. Consequently, an aggregate data rate of 200Gb/s over 70 meters transmission can be achieved by this product, to support the ultra-fast computing data exchange.

The product is designed with form factor, optical/electrical connection according to the QSFP56 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Description

This product converts the parallel electrical input signals into parallel optical signals (light), by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The light propagates through multimode fibers inside the fiber cable individually and is captured by the photo diode array. The optical signals are converted into parallel electrical signals and outputted. Consequently, each terminal of the cable has 8 ports, 4 for data transmission and 4 for data receiving, to provide totally 200Gb/s data exchange. Figure 1 shows the functional block diagram of the parallel AOC.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used. Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

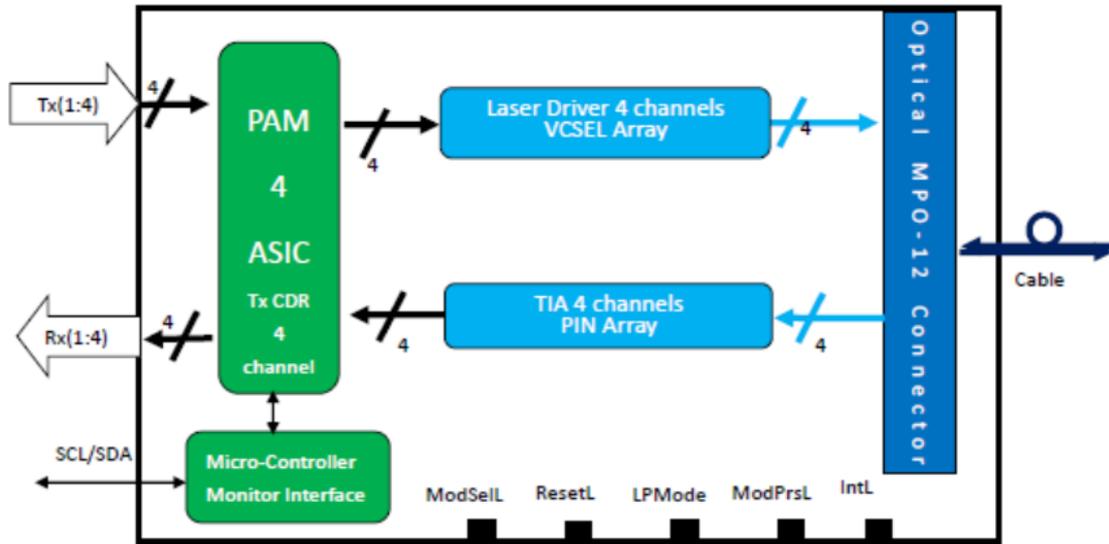
The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Initialize Mode (InitMode) is an input signal. It is pulled up to Vcc in the QSFP56 module. The InitMode signal allows the host to define whether the QSFP56 module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP56 Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max	Unit
Storage Temperature	T_S	-40	85	°C
Operating Case Temperature	T_{OP}	0	70	°C
Power Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (non-condensation)	RH	0	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max	Unit	Note
Operating Case Temperature	T_{OP}	0		70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4×10^{-4}		
Post-FEC Bit Error Ratio				1×10^{-12}		1
Link Distance with OM3	D	0.5		70	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Digital Diagnostic Functions

Parameter	Symbol	Min	Max	Unit	Note
Temperature monitor absolute error	<i>DMI_Temp</i>	-3	3	°C	Over operating temperature range
Supply voltage monitor absolute error	<i>DMI_VCC</i>	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	<i>DMI_RX_Ch</i>	-2	2	dB	1
Channel Bias current monitor	<i>DMI_Ibias_Ch</i>	-10%	10%	mA	
Channel TX power monitor absolute error	<i>DMI_TX_Ch</i>	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different fibers, there could be an additional +/- 1 dB fluctuation, or a +/- 3 dB total accuracy.

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Power Consumption				5	W	
Supply Current	<i>I_{cc}</i>			1.52	A	

Transmitter Electrical Characteristics (each lane)

Parameter	Symbol	Min	Typical	Max	Unit	Note
Signaling Rate, each Lane	<i>TP1</i>	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	<i>TP1a</i>	900			mVpp	1
Differential Termination Mismatch	<i>TP1</i>			10	%	
Differential Input Return Loss	<i>TP1</i>	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	<i>TP1</i>	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	<i>TP1a</i>	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	<i>TP1a</i>	-0.4 to 3.3			V	
DC Common Mode Input Voltage	<i>TP1</i>	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

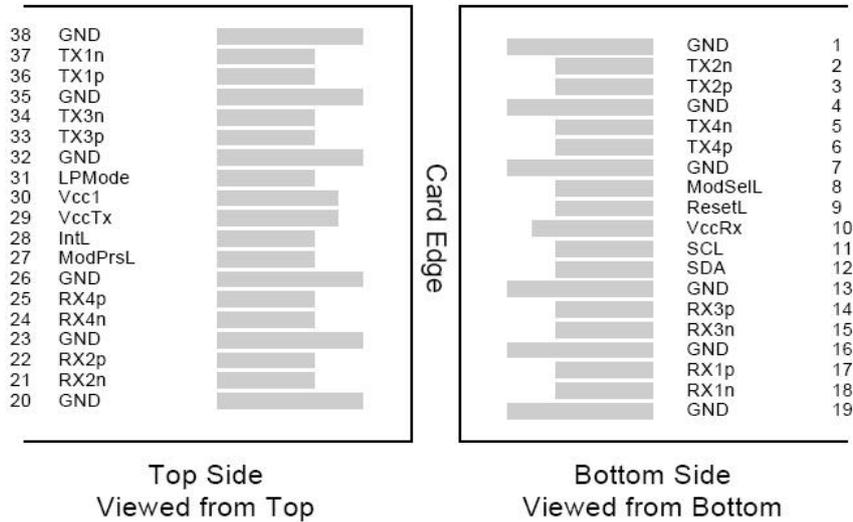
Transmitter Optical Characteristics (each lane)

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typical</i>	<i>Max</i>	<i>Unit</i>	<i>Note</i>
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
Common Mode vOLTAGE		-350		2850	mV	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	1

Notes:

- DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Pin Assignment



Pin Description

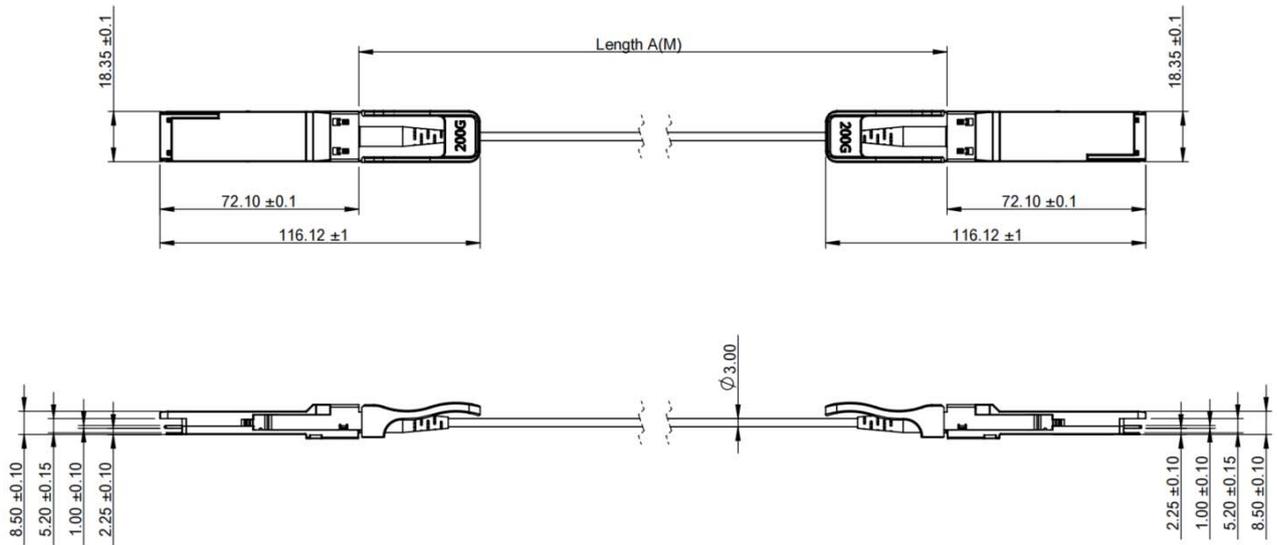
Pin	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	

Pin	Logic	Symbol	Name/Description	Note
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

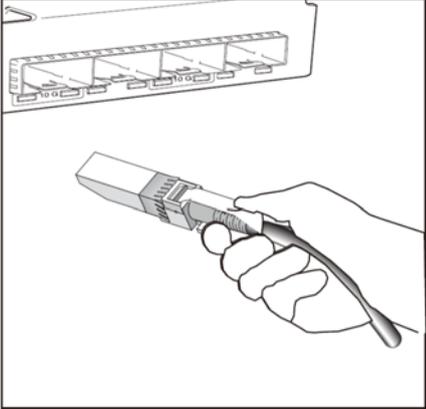
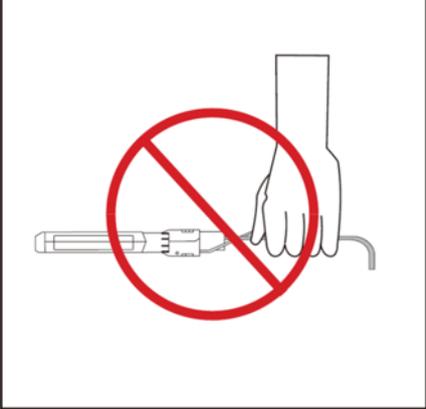
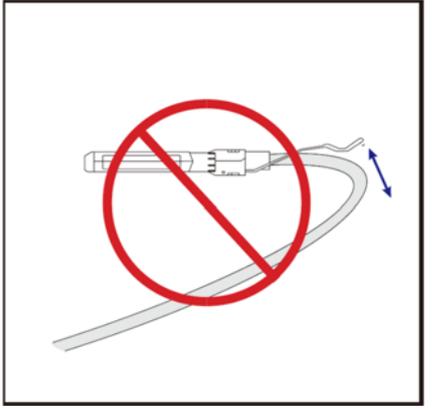
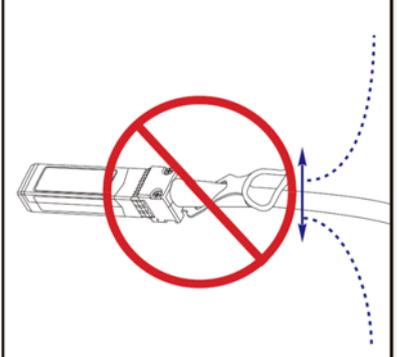
Notes:

- GND is the symbol for signal and supply (power) common for QSFP56 modules. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
- VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP56 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Dimensions



Important Notice

		
<p>Holding the SFP+ connector by its sides, insert the connector into the port on the switch</p>	<p>Do not handle by cable</p>	<p>DO NOT Over-bend the cable behind the connector</p>
		
<p>DO NOT twist the cable</p>	<p>DO NOT kink the cable</p>	<p>DO NOT bend up and down the cable</p>

Ordering Information

<i>Model Number</i>	<i>Part Number</i>	<i>Length(M)</i>	<i>Voltage</i>	<i>Temperature</i>
200G QSFP56 AOC	OPQS56-F-03-AKT	3	3.3V	0°C to 70 °C
200G QSFP56 AOC	OPQS56-F-05-AKT	5	3.3V	0°C to 70 °C
200G QSFP56 AOC	OPQS56-F-07-AKT	7	3.3V	0°C to 70 °C
200G QSFP56 AOC	OPQS56-F-10-AKT	10	3.3V	0°C to 70 °C
200G QSFP56 AOC	OPQS56-F-20-AKT	20	3.3V	0°C to 70 °C
200G QSFP56 AOC	OPQS56-F-30-AKT	30	3.3V	0°C to 70 °C

Modification History

<i>Revision</i>	<i>Date</i>	<i>Description</i>
A1	Sep. 2021	Initial Release

Note: All information contained in this document is subject to change without notice.