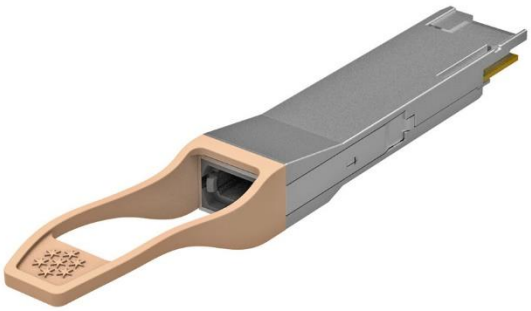


Features

- 8 channels full-duplex transceiver modules
- Transmission data rate up to 26Gbps per channel
- 8 channels 850nm VCSEL array
- 8 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <4W
- Hot Pluggable QSFP DD form factor
- Maximum link length of 70m on OM3 Multimode Fiber (MMF) and 100m on OM4 MMF
- MPO24 connector receptacle
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant(lead free)

Applications

- IEEE 802.3bm 100GBASE SR4

Absolute Maximum Ratings

Parameter	*Symbol*	*Min.*	*Max.*	*Units*
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V
Storage Temperature	*Tst*	-20	85	ºC
Case Operating Temperature	*Top*	0	70	ºC
Humidity (non-condensing)	*Rh*	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage	*Vcc*	3.13	3.3	3.47	V
Operating Case Temperature	*Tca*	0		70	ºC
Data Rate Per Lane	*fd*		25.78125		Gb/s
Humidity	*Rh*	5		85	%
Power Dissipation	*Pm*			4	W

Electrical Specifications

Parameter	Symbol	Min.	Tpy.	Max.	Units	Note
Differential input impedance	Z_{in}	90	100	110	ohm	
Differential Output impedance	Z_{out}	90	100	110	ohm	
Differential input voltage Amplitude	ΔV_{in}	300		1100	mVp-p	
Differential output voltage Amplitude	ΔV_{out}	500		800	mVp-p	
Skew	*Sw*			300	ps	
Bit Error Rate	*BER*			5E-5		
Input Logic Level High	V_{IH}	2.0		V_{CC}	V	
Input Logic Level Low	V_{IL}	0		0.8	V	
Output Logic Level High	V_{OH}	V_{CC}-0.5		V_{CC}	V	
Output Logic Level Low	V_{OL}	0		0.4	V	

Notes:

1. BER=5E-5; PRBS 2^31-1@25.78125Gbps. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Transmitter Electro-Optical Characteristics

***Vcc* = 3.13 V to 3.47 V, T_C = 0 °C to 70 °C**

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*	*Notes*
Centre Wavelength	λc	840	850	860	nm	-
RMS spectral width	$\Delta\lambda$	-	-	0.6	nm	
Average launch power, each lane	P_{out}	-8.4	-	2.4	dBm	-
Optical Modulation Amplitude	*OMA*	-6.4		3	dBm	-
(OMA),each lane	*TDEC*			4.3	dB	
Transmitter and dispersion eye closure(TDEC),each lane	*ER*	3	-	-	dB	-
Extinction Ratio				-30	dB	-
Average launch power of OFF transmitter, each lane	λc	840	850	860	nm	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		SPECIFICATION VALUES {0.3,0.38,0.45,0.35,0.41.0.5}				Hit Ratio = $5x10^{-5}$

Receiver Electro-Optical Characteristics

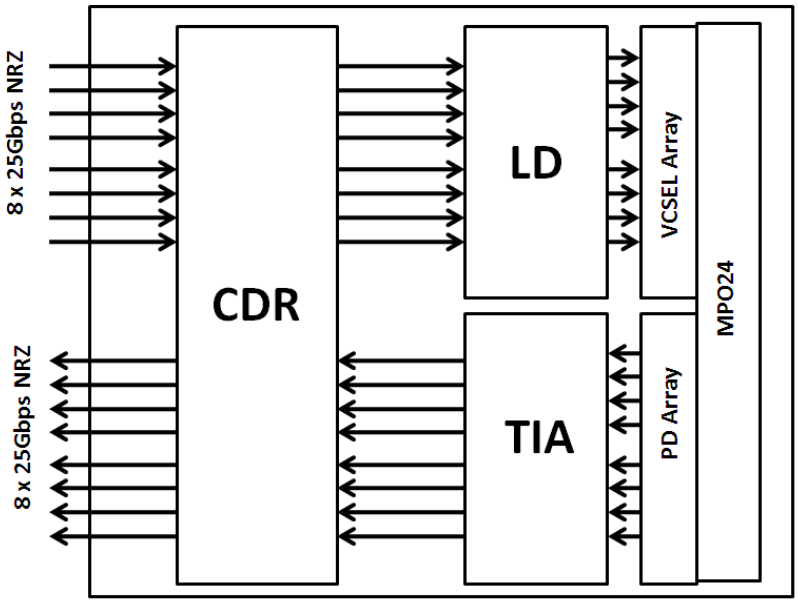
***Vcc* = 3.13 V to 3.47 V, T_C = 0 °C to 70 °C**

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*	*Notes*
Centre Wavelength	λc	840	850	860	nm	
Stressed receiver sensitivity in OMA				-5.2	dBm	1
Maximum Average power at receiver , each lane input, each lane				2.4	dBm	
Minimum Average power at receiver , each lane				-10.3	dBm	
Receiver Reflectance				-12	dB	
LOS Assert		-30			dBm	
LOS De-Assert – OMA				-7.5	dBm	
LOS Hysteresis		0.5			dB	

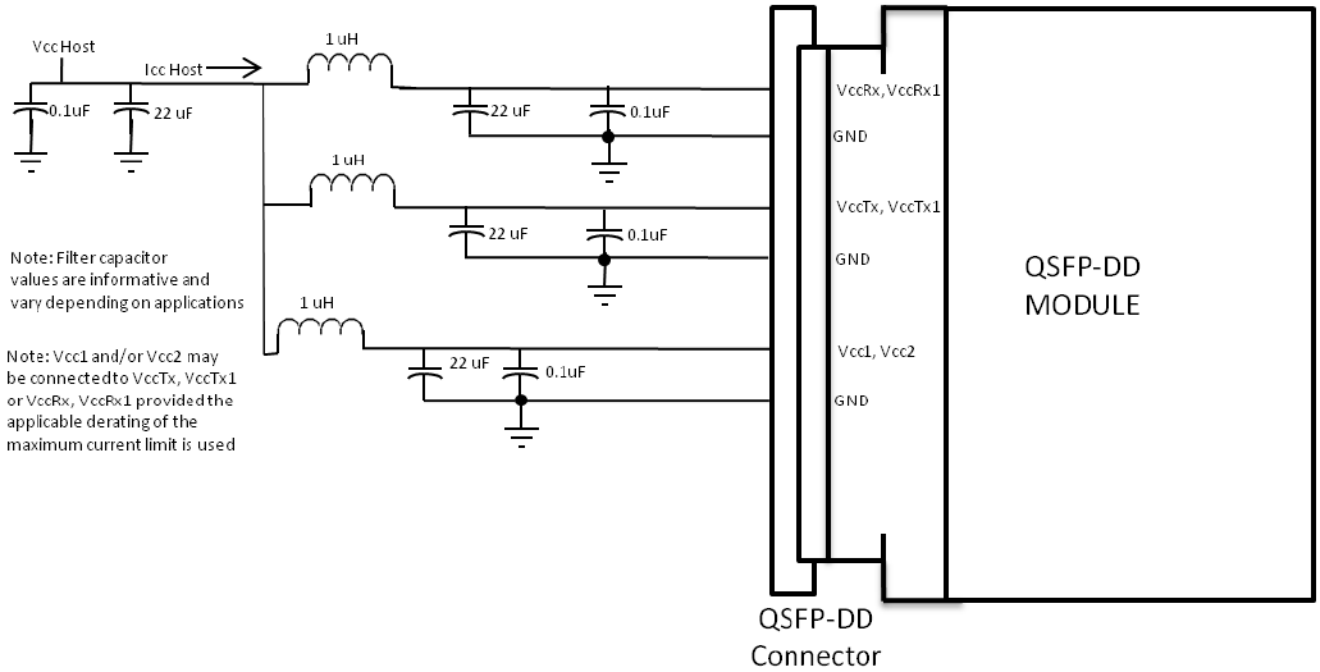
Note：

1. Measured with conformance test signal at TP3 for BER = 5E-5 Per-FEC

Block Diagram

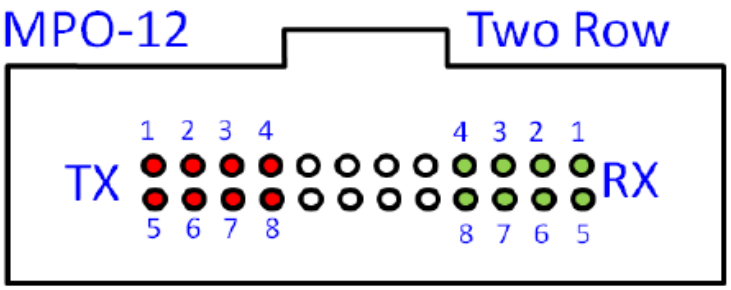


Power Supply Filtering

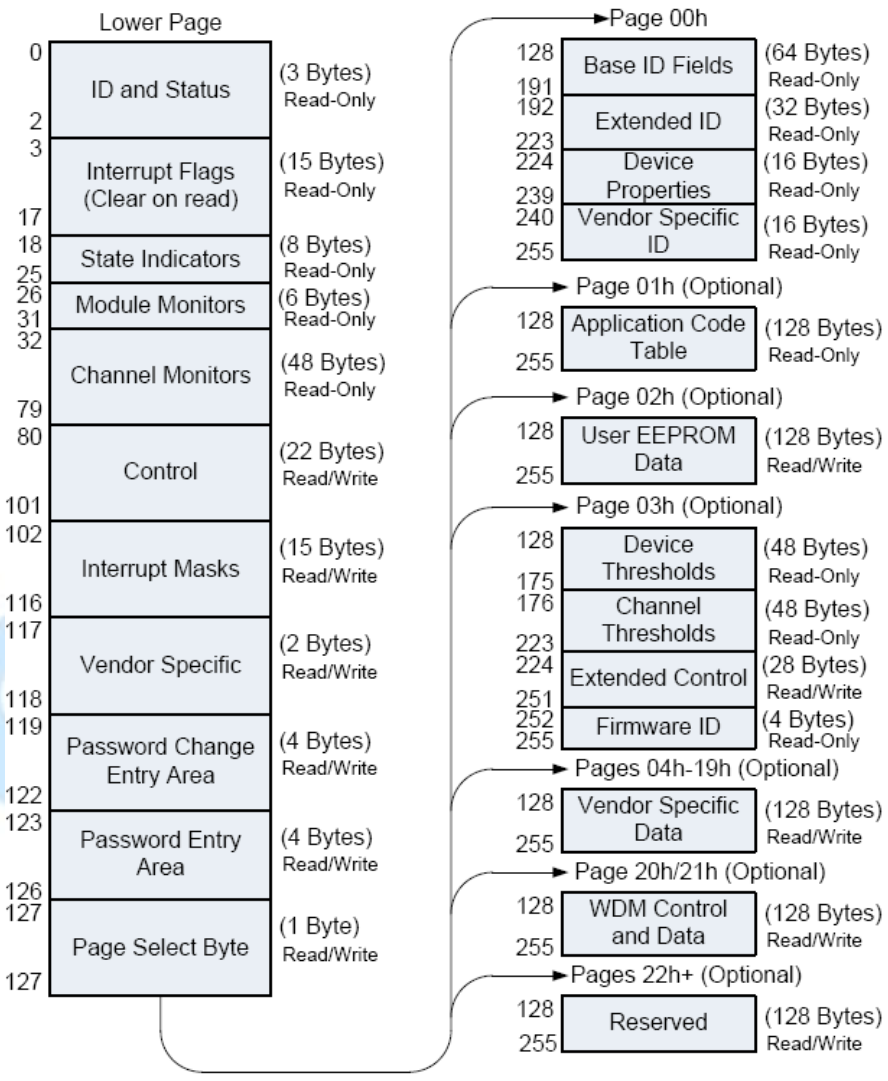


Optical Interface Lanes and Assignment

The optical interface port is a male MPO24 connector .



QSFP DD Memory Map



Low Memory Map

Address	Description	Type
0 - 2	Id and Status (3 bytes)	Read-only
3 - 17	Interrupt Flags (15 bytes)	Read-only
18 - 25	State Indicators (8 bytes)	Read-only
26 - 31	Module card Monitors (6 bytes)	Read-only
32 - 79	Channel Monitors (48 bytes)	Read-only
80 - 101	Control Fields (22 bytes)	Read/Write
102 - 116	Interrupt Flag Masks (15 bytes)	Read/Write
117 - 118	Reserved	Read/Write
119 - 122	Password Change Area (4 bytes)	Write-Only
123 - 126	Password Entry Area (4 bytes)	Write-Only
127	Page Select Byte	Read/Write

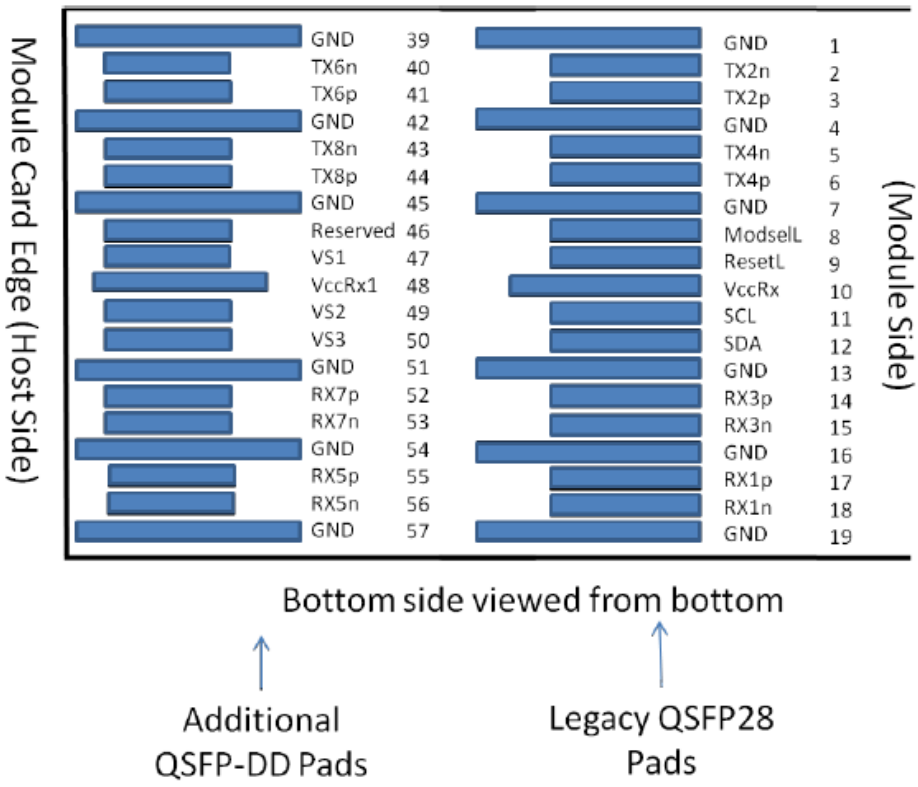
Page 00 Memory Map

Address	Size (bytes)	Name	Description
Base ID Fields:			
128	1	Identifier	Identifier Type of module
129	1	Ext. Identifier	Extended Identifier
130	1	Connector Type	Code for media connector type
131-138	8	Specification compliance	Code for electronic compatibility or optical compatibility
139	1	Encoding	Code for serial encoding algorithm
140	1	BR, nominal	Nominal bit rate, units of 100 MBits/s
141	1	Extended rate select compliance	Tags for extended rate select compliance
142-146	5	Link length	Link length / transmission media
147	1	Device technology	Device technology
148-163	16	Vendor name	Vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand
165-167	3	Vendor OUI	Vendor IEEE company ID
168-183	16	Vendor PN	Part number provided by vendor (ASCII)
184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
186-187	2	Wavelength or Copper	Nominal laser wavelength
		cable Attenuation	(wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5GHz (Adrs 186) and 5.0GHz (Adrs 187)
188-189	2	Wavelength tolerance	Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tolerance=value/200 in nm)
190	1	Max case temp.	Maximum case temperature in degrees C
191	1	CC_BASE	Check code for base ID fields (addresses 128-190 inclusive)
Extended ID Fields:			
192-195	4	Options	Indicates which optional capabilities are implemented in the module
196-211	16	Vendor S/N	Vendor product serial number
212-219	8	Date Code	Vendor's manufacturing date code
220	1	Diagnostic Monitoring Type	Indicates which types of diagnostic monitoring are implemented in the module
221-222	2	Enhanced Options	Indicates which optional enhanced features are implemented in the module.
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222 inclusive)
224-238	15	Device Properties	Provides detailed information about the device
239	1	CC-PROP	Check code for the Device Properties Fields (addresses 224-2382 inclusive)
Vendor Specific ID Fields:			
240-255	16	Vendor-Specific	Vendor-specific ID information

Timing for Soft Control and Status Functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[2], hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	2		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[3] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Deassert Time (optional fast mode)	toff_losf		3	ms	Time from signal present to negation of Rx LOS status bit.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[1] until associated IntL operation resumes
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Note 1. Measured from the rising edge of SDA in the stop bit of the write transaction					
Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.					
Note 3. Measured from the rising edge of SDA in the stop bit of the read transaction					

Pin Assignment



ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Optech QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Pin Description

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

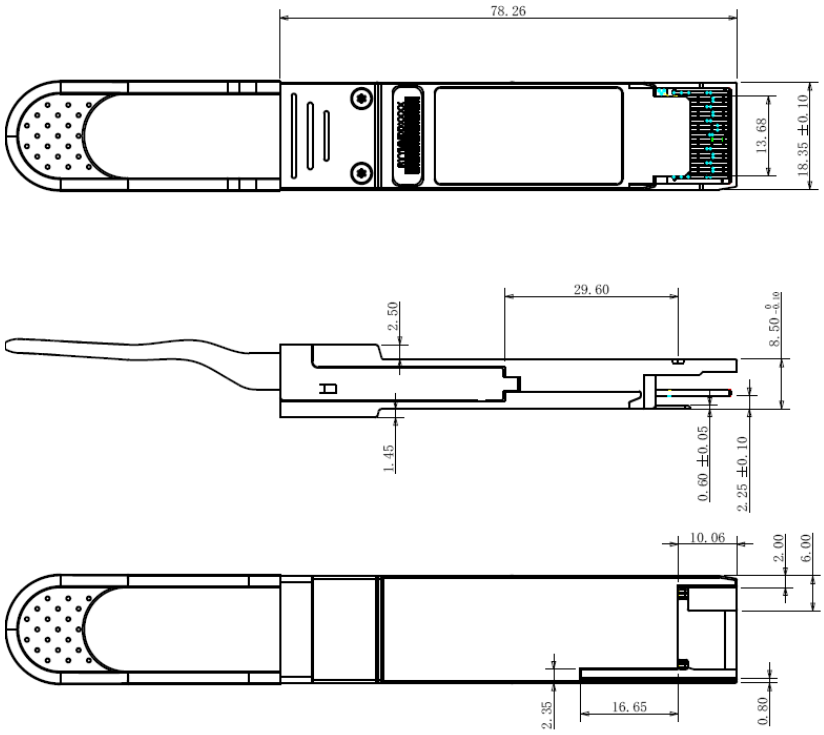
Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

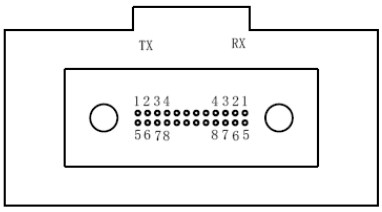
Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Dimensions


78.26
13.68
18.35 ±0.10
29.60
2.50
8.50
1.45
0.60 ±0.05
2.25 ±0.10
10.06
2.00
6.00
2.35
16.65
0.80

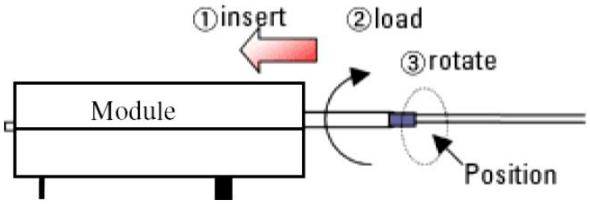

TX
RX
1 2 3 4
5 6 7 8
4 3 2 1
8 7 6 5

Optical Receptacle Cleaning Recommendations :

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.

Cleaning of patch-cord

Cleaning of fiber stub



1. Insert
   Ensure that stick is held straight when inserting into sleeve.
2. Load
   Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve.
3. Rotate
   Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained.

Notice: Number of possible wipes:
Maintenance (repair) ~1 use / piece
Equipment construction: 4 uses / piece (max.)

Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information

OP D V - M X1 - 85 - C F

Product Code:
5=GBIC;
6=SFP-LC;
7=XFP;
8=XENPAK;
9=X2;
A=SFP+ (SFP28);
C=QSFP+ (QSFP28);
D=QSFP-DD;
O=OSFP;
F=CFP;
G=CFP2;
H=CFP4;
J=CXP;
P=SFP-SC;
Q=SFP-MTRJ

Data Rate:
A=155Mb/s;
B=622Mb/s;
C=1.25Gb/s
(1000Base for Copper-T);
D=2.125Gb/s;
E=2.5Gb/s;
F=4.25Gb/s;
G=3.1Gb/s;
J=2.97G
P=6.144G:
Q=7.37G;
H=8.5Gb/s;
K=10Gb/s;
T=1/10Gb/s (10/100/1000Base for Copper-T);
L=16Gb/s;
R=20Gb/s;
X=25Gb/s;
Z=32Gb/s;
S=40Gb/s;
U=56Gb/s;
W=100Gb/s (4x25G or 10x10G);
V=200Gb/s;
Y=400Gb/s;
M=100Base-X SGMII;
N=100/1000Base-X SGMII

Type:
S=Single-mode;
M=Multi-mode;
W=BWDM;
B=DUAL-BWDM;
C=CWDM;
D=DWDM;
T=Copper-T (RJ-45)
E=GEPON ONU;
F=GEPON OLT;
G=GPON ONU;
H=GPON OLT
X=MMF/SMF

Reach:
Normal:
X1=Under 150m;
X2=220m;
X3=300m;
X5=550m;
02=2km,
10=10km;
70=70km;
A0=100km;
C0=120km
CWDM:
20=20dB;
24=24dB;
28=28dB

Wavelength:
Normal:
85=850nm;
13=1310nm;
15=1550nm;
00=Copper T (RJ-45)

CWDM:
27=1270nm;
47=1470nm;
61=1610nm

BWDM:
B3=Tx1310/Rx1550; B5=Tx1550/Rx1310;
B4=Tx1310/Rx1490; B9=Tx1490/Rx1310;
51=Tx1510/Rx1570; 57=Tx1570/Rx1510;
27=Tx1270/Rx1330; 33=Tx1330/Rx1270;
B2=Tx1270/Rx1577; B7=Tx1577/Rx1270
T2=2TX1310nm; T3=TX1310nm;
T5=TX1550nm

DWDM:
17=Channel 17
34= Channel 34
00=Channel 17~61 Tunable

Operating Temperature:
C=Commercial Purpose
(0~70℃);
I= Industrial Purpose
(Extended Range)

For Optech Internal Ref.

Model Number	*Part Number*	*Reach*	*Voltage*	*Temperature*
QSFP-DD-200G-SR8	OPDV-MX1-85-CF	70m on OM3 / 100m on OM4	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.