Features

- 8 channels full-duplex transceiver modules
- Supports 8x25Gb/s aggregate bit rates
- Supports 8x10Gb/s aggregate bit rates if required
- 8 channels 1310nm DFB
- 8 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption<6W
- Hot Pluggable QSFP DD form factor
- Up to 2km reach for G.652 SMF
- Single male MPO(APC 8-degree) connector receptacle
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 2.0 compliant(lead free)

Applications

- 2x100G Ethernet links
- Infiniband DDR/EDR
- Data Center and Enterprise networking

Absolute Maximum Ratings

Parameter	*Symbol*	*Min.*	*Max.*	*Units*
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V
Storage Temperature	T_s	-20	85	ºC
Case Operating Temperature	T_c	0	70	ºC
Humidity (non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tc	0		70	ºC
Data Rate Per Lane	fd	10.3125	25.78125		Gb/s
Humidity	Rh	5		85	%
Power Dissipation	Pm		5.28	6	W
Fiber Bend Radius	Rb	0.002		2	km

Transmitter Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Input Logic Level High	V_{IH}	2.0		Vcc	V	
Input Logic Level Low	V_{IL}	0		0.8	V	
Differential Input Voltage Amplitude[1]	V_{in}	190		700	mVp-p	-
Differential Input Impedance	Z_{in}	90	100	110	Ohm	-
Center Wavelength	λc	1295	1310	1325	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power (each lane)	P_{AVG}	-6		2	dBm	
Optical Modulation Amplitude (each lane)	P_{OMA}	-5.0		2.2	dBm	
Transmitter and Dispersion Penalty (TDP) (each lane)	TDP			2.9	dB	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	T_{OL}			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Average Launch Power of OFF transmitter (each lane)	P_{OFF}			-30	dBm	
Eye Mask Coordinates: X1, X2, X3, Y1, Y2, Y3	{0.31,0.4,0.45,0.34,0.38.0.4}			Hit Ratio = 5x10-5		

Note:

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. Even if the TDP <1dB, the OMA min must exceed the minimum value specified here.
3. Sensitivity is specified at 5x10^-5 BER at 25.78125Gb/s.

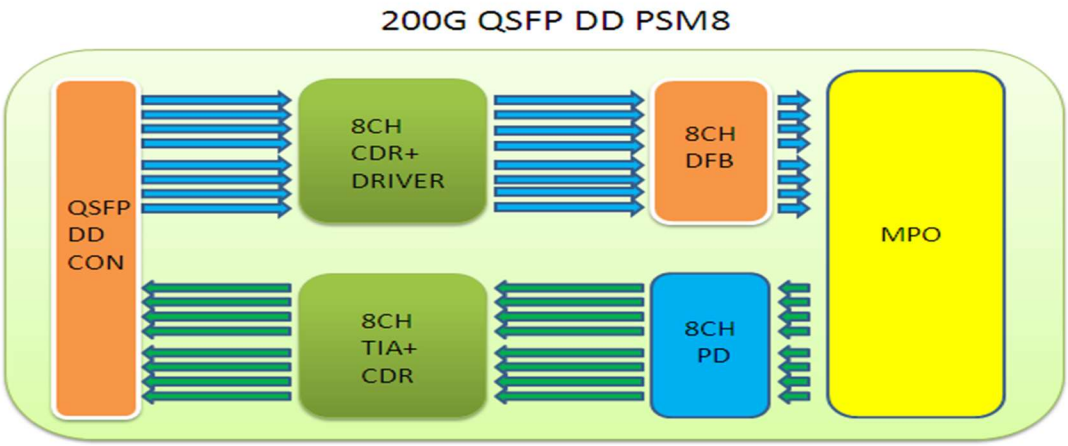
Receiver Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Output Logic Level High	V_{OH}	V_{cc}-0.5		Vcc	V	
Output Logic Level Low	V_{OL}	0		0.4	V	
Differential Output Voltage Swing	V_{out}	300		850	mVp-p	
Differential Output Impedance	Z_{out}	90	100	110	Ohm	
Damage Threshold (each lane)	TH_d	3.0			dBm	1
Average Receive Power (each lane)		-12.66		2.0	dBm	
Receive Power (OMA) (each lane) (max)				2.2	dBm	
Receiver Sensitivity (OMA) (each lane)	SEN			-11.35	dBm	
Receive Reflectance	RR			-26	dBm	
LOS Assert	LOSA		-18		dBm	
LOS De-Assert – OMA	LOSD		-15		dBm	
LOS Hysteresis	LOSH	0.5		3	dB	

Note：

1. Even if the TDP<1dB,the OMA min must exceed the minimum value specified here .
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
3. Sensitivity is specified at $5x10^{-5}$ @25.78125Gbps.

Block Diagram



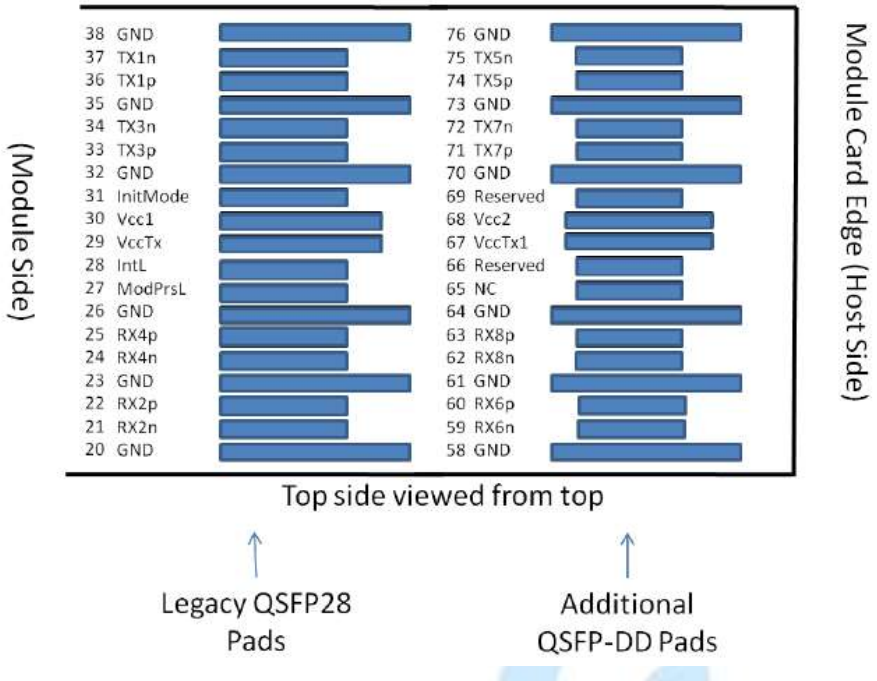
Pin Assignment

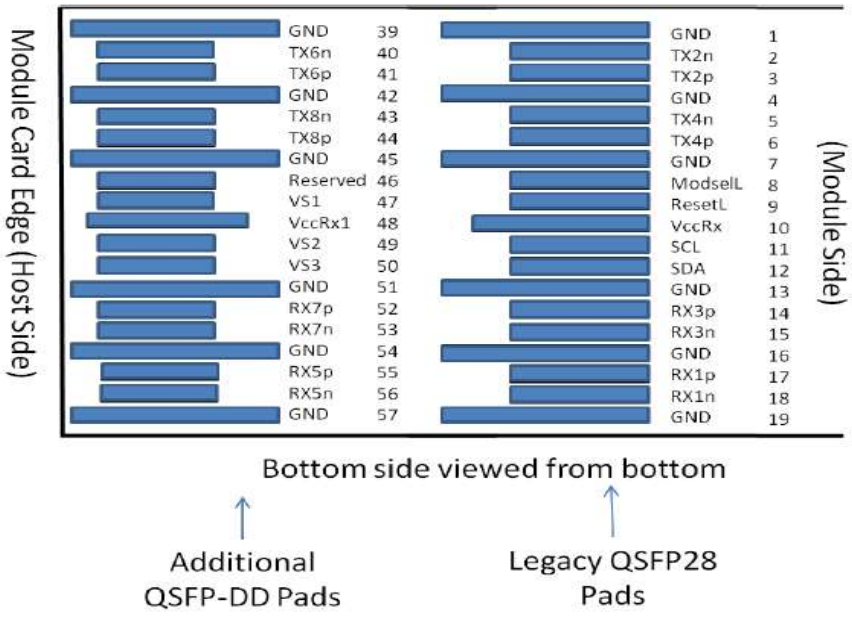
Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1


(Module Side)
38 GND
37 TX1n
36 TX1p
35 GND
34 TX3n
33 TX3p
32 GND
31 InitMode
30 Vcc1
29 VccTx
28 IntL
27 ModPrsL
26 GND
25 RX4p
24 RX4n
23 GND
22 RX2p
21 RX2n
20 GND
76 GND
75 TX5n
74 TX5p
73 GND
72 TX7n
71 TX7p
70 GND
69 Reserved
68 Vcc2
67 VccTx1
66 Reserved
65 NC
64 GND
63 RX8p
62 RX8n
61 GND
60 RX6p
59 RX6n
58 GND
Module Card Edge (Host Side)
Top side viewed from top
Legacy QSFP28 Pads
Additional QSFP-DD Pads


Module Card Edge (Host Side)
GND 39
TX6n 40
TX6p 41
GND 42
TX8n 43
TX8p 44
GND 45
Reserved 46
VS1 47
VccRx1 48
VS2 49
VS3 50
GND 51
RX7p 52
RX7n 53
GND 54
RX5p 55
RX5n 56
GND 57
GND 1
TX2n 2
TX2p 3
GND 4
TX4n 5
TX4p 6
GND 7
ModselL 8
ResetL 9
VccRx 10
SCL 11
SDA 12
GND 13
RX3p 14
RX3n 15
GND 16
RX1p 17
RX1n 18
GND 19
(Module Side)
Bottom side viewed from bottom
Additional QSFP-DD Pads
Legacy QSFP28 Pads

ModSelL Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 13) initiates a complete module reset, returning all user module settings to their default state.

InitMode Pin

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in Section 7.5. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for signal description.

MoPrsL Pin

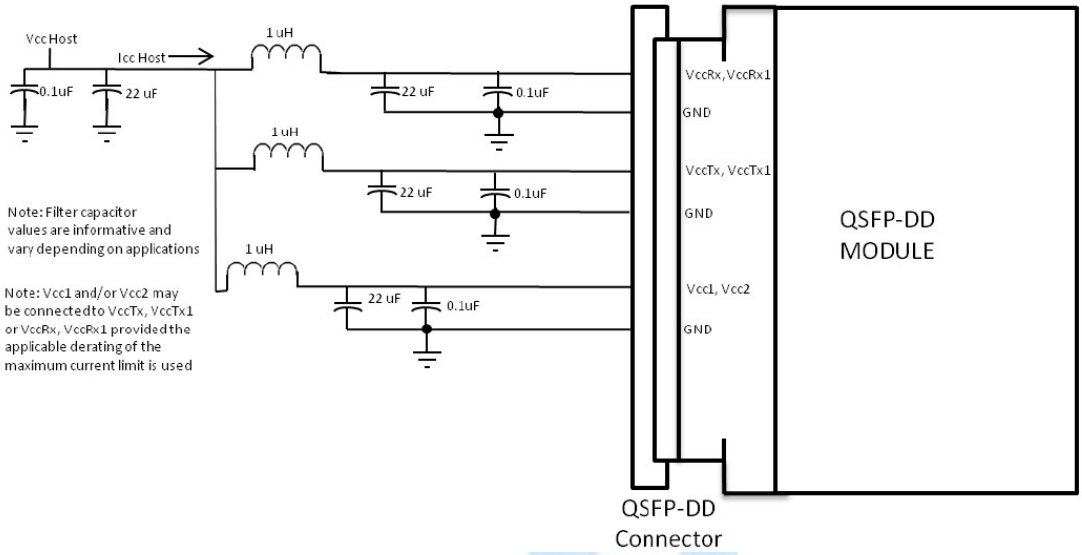
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

Power Supply Filtering

The host boards should use the power supply filtering shown in Figure 3.



Optical Interface Lanes and Assignment

The optical interface port is an male MPO24 connector.

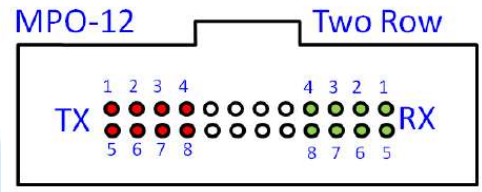


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Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Optech QSFP DD products. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to address in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

The interface address used is A0xh and is mainly used for time critical data like interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

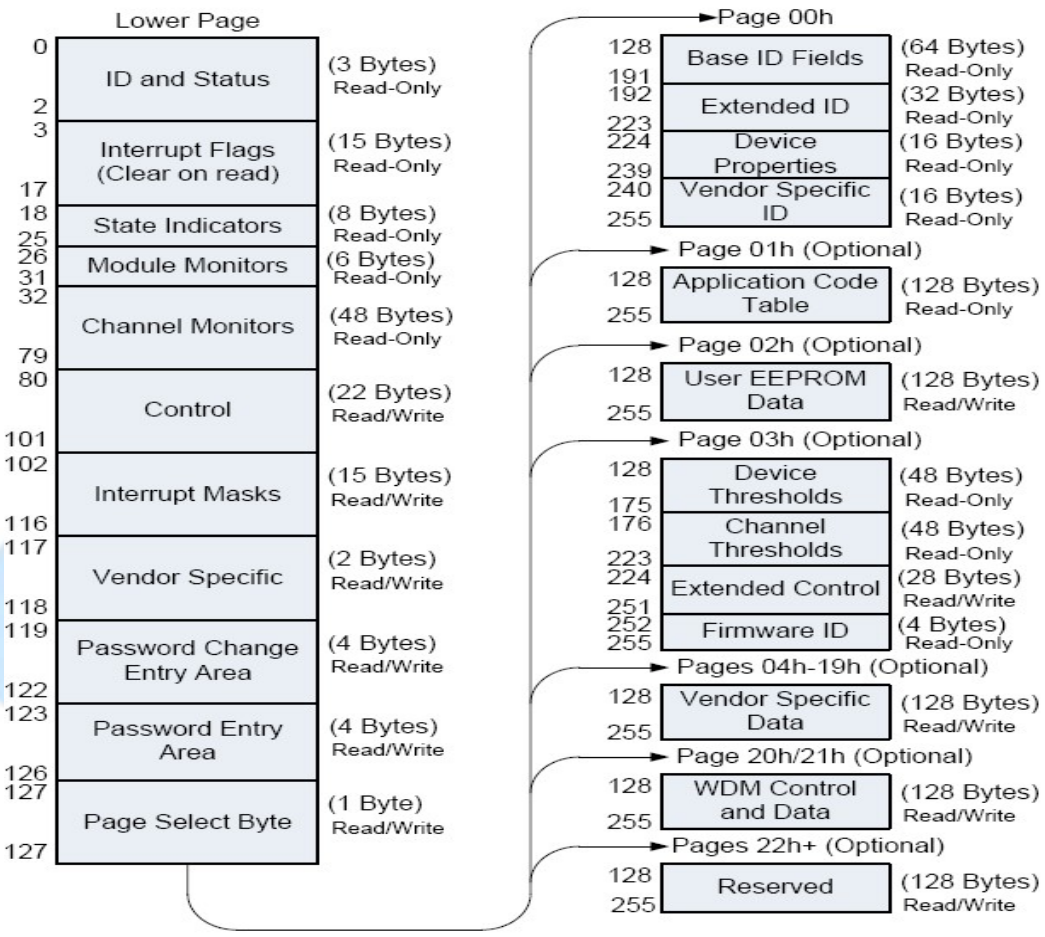


Figure 5. QSFP28 Memory Map

Table 16- Lower Page Overview (Lower Page)

Address	Description	Type
0 - 2	Id and Status (3 bytes)	Read-only
3 - 17	Interrupt Flags (15 bytes)	Read-only
18 - 25	State Indicators (8 bytes)	Read-only
26 - 31	Module card Monitors (6 bytes)	Read-only
32 - 79	Channel Monitors (48 bytes)	Read-only
80 - 101	Control Fields (22 bytes)	Read/Write
102 - 116	Interrupt Flag Masks (15 bytes)	Read/Write
117 - 118	Reserved	Read/Write
119 - 122	Password Change Area (4 bytes)	Write-Only
123 - 126	Password Entry Area (4 bytes)	Write-Only
127	Page Select Byte	Read/Write

Table 28- Upper Page 0 Overview (Page 00h)

Address	Size (bytes)	Name	Description
Base ID Fields:			
128	1	Identifier	Identifier Type of module
129	1	Ext. Identifier	Extended Identifier
130	1	Connector Type	Code for media connector type
131-138	8	Specification compliance	Code for electronic compatibility or optical compatibility
139	1	Encoding	Code for serial encoding algorithm
140	1	BR, nominal	Nominal bit rate, units of 100 MBits/s
141	1	Extended rate select compliance	Tags for extended rate select compliance
142-146	5	Link length	Link length / transmission media
147	1	Device technology	Device technology
148-163	16	Vendor name	Vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand
165-167	3	Vendor OUI	Vendor IEEE company ID
168-183	16	Vendor PN	Part number provided by vendor (ASCII)
184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
186-187	2	Wavelength or Copper	Nominal laser wavelength

Figure 6. Low Memory Map

		cable Attenuation	(wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5GHz (Adrs 186) and 5.0GHz (Adrs 187)
188-189	2	Wavelength tolerance	Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tolerance=value/200 in nm)
190	1	Max case temp.	Maximum case temperature in degrees C
191	1	CC_BASE	Check code for base ID fields (addresses 128-190 inclusive)
Extended ID Fields:			
192-195	4	Options	Indicates which optional capabilities are implemented in the module
196-211	16	Vendor S/N	Vendor product serial number
212-219	8	Date Code	Vendor's manufacturing date code
220	1	Diagnostic Monitoring Type	Indicates which types of diagnostic monitoring are implemented in the module
221-222	2	Enhanced Options	Indicates which optional enhanced features are implemented in the module.
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222 inclusive)
224-238	15	Device Properties	Provides detailed information about the device
239	1	CC-PROP	Check code for the Device Properties Fields (addresses 224-2382 inclusive)
Vendor Specific ID Fields:			
240-255	16	Vendor-Specific	Vendor-specific ID information

Figure 7. Page 00 Memory Map

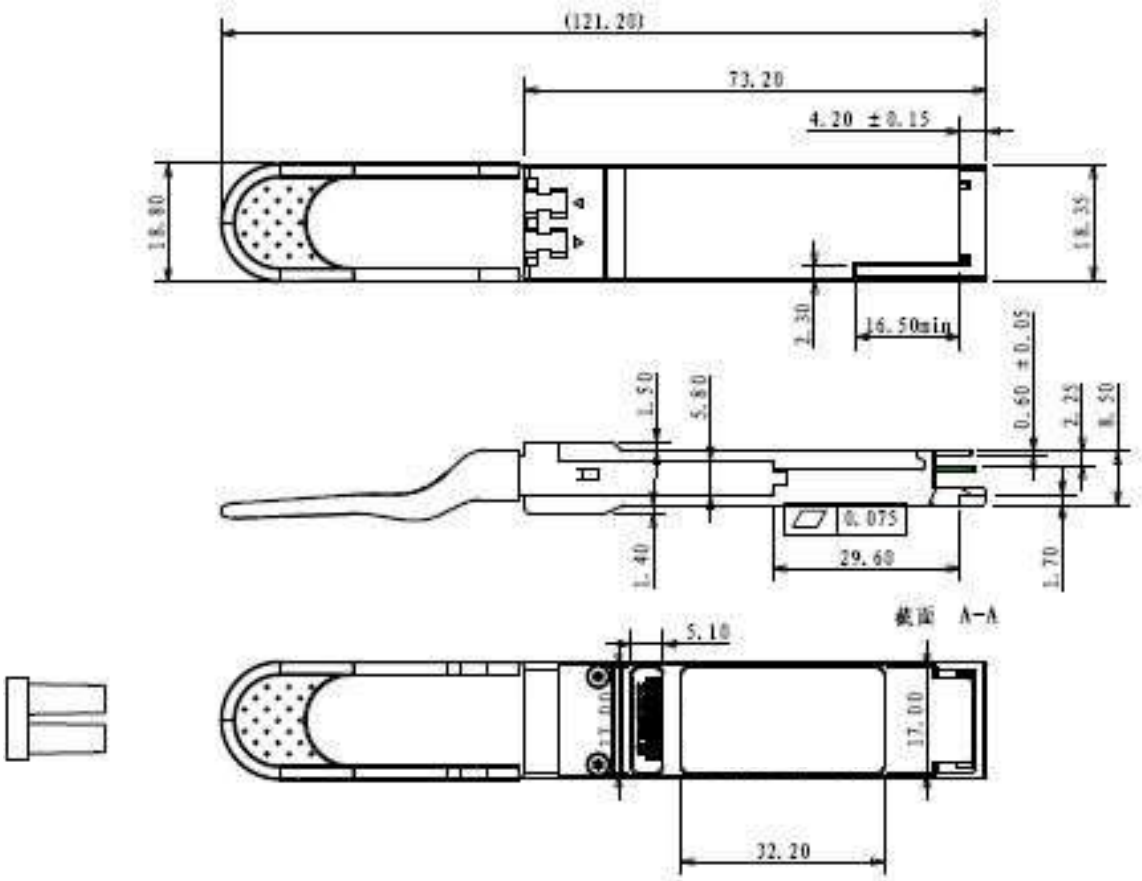
Timing for Soft Control and Status Functions

Table 13- Timing for QSFP-DD soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[2], hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	2		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[3] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Deassert Time (optional fast mode)	toff_losf		3	ms	Time from signal present to negation of Rx LOS status bit.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[1] until associated IntL operation resumes
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Note 1. Measured from the rising edge of SDA in the stop bit of the write transaction					
Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.					
Note 3. Measured from the rising edge of SDA in the stop bit of the read transaction					

Figure8. Timing Specifications

Dimensions

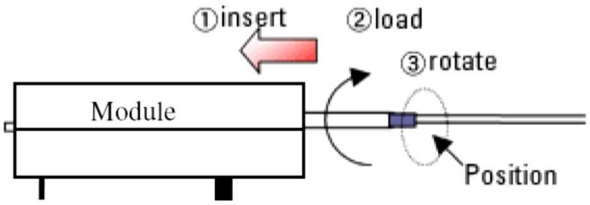

(121.20)
73.20
4.20 ±0.15
18.80
18.35
2.30
16.50min
0.60 ±0.05
2.25
8.50
1.50
5.60
0.075
29.60
1.40
1.70
截面 A-A
5.10
17.00
17.00
32.20

Optical Receptacle Cleaning Recommendations :

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.

Cleaning of patch-cord

Cleaning of fiber stub



1. Insert
   Ensure that stick is held straight when inserting into sleeve.
2. Load
   Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve.
3. Rotate
   Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained.

Notice: Number of possible wipes:
Maintenance (repair) ~1 use / piece
Equipment construction: 4 uses / piece (max.)

Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information

OP C W - S 30 - 13 - C F T

Product Code:
5=GBIC;
6=SFP-LC;
7=XFP;
8=XENPAK;
9=X2;
A=SFP+ (SFP28);
C=QSFP+ (QSFP28);
F=CFP;
G=CFP2;
H=CFP4;
P=SFP-SC;
Q=SFP-MTRJ

Data Rate:
A=155Mb/s;
B=622Mb/s;
C=1.25Gb/s;
D=2.125Gb/s;
E=2.5Gb/s;
F=4.25Gb/s;
G=3.1Gb/s;
J=2.97G
P=6.144G:
Q=7.37G;
H=8.5Gb/s;
K=10Gb/s;
T=1/10Gb/s
L=16Gb/s;
R=20Gb/s;
X=25Gb/s;
S=40Gb/s;
U=56Gb/s;
W=100Gb/s (4x25G or 10x10G);
M=100Base-X SGMII;
N=100/1000Base-X SGMII;

Type:
S=Single-mode;
M=Multi-mode;
W=BWDM;
B=DUAL-BWDM;
C=CWDM;
D=DWDM;
T=Copper-T (RJ-45)
E=GEPON ONU;
F=GEPON OLT;
G=GPON ONU;
H=GPON OLT
X=MMF/SMF

Reach:
Normal:
X1=Under 150m;
X2=220m;
X3=300m;
X5=550m;
02=2km,
10=10km;
70=70km;
A0=100km;
C0=120km

CWDM:
20=20dB;
24=24dB;
28=28dB

Wavelength:
Normal:
85=850nm;
13=1310nm;
15=1550nm;
00=Copper T (RJ-45)

CWDM:
27=1270nm;
47=1470nm;
61=1610nm

BWDM:
B3=Tx1310/Rx1550; B5=Tx1550/Rx1310;
B4=Tx1310/Rx1490; B9=Tx1490/Rx1310;
51=Tx1510/Rx1570; 57=Tx1570/Rx1510;
27=Tx1270/Rx1330; 33=Tx1330/Rx1270;
B2=Tx1270/Rx1577; B7=Tx1577/Rx1270
T2=2TX1310nm; T3=TX1310nm;
T5=TX1550nm

DWDM:
17=Channel 17
34= Channel 34
00=Channel 17~61 Tunable

Operating Temperature:
C=Commercial Purpose
(0~70℃);
I= Industrial Purpose
(Extended Range)

For Optech Internal Ref.

Model Number	*Part Number*	*Reach*	*Voltage*	*Temperature*
QSFP-DD-200G-PSM8	OPDV-S02-13-CFS	2km	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.