Features

- OSFP MSA compliant
- Parallel 4 Optical Lanes
- IEEE802.3bs Specification compliant
- 100G Single Lambda 100G-FR compliant
- Minimum 8dB Link Budget at Minimum 5dB Channel loss
- Up to 2km transmission on single mode fiber (SMF) with FEC
- Operating case temperature: 0~70°C
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel.

Applications

- 400G Ethernet
- Infiniband interconnects
- Datacenter Enterprise networking

Description

This product is a 400Gb/s Octal Small Form-factor Pluggable (OSFP) optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation fo ran aggregate data rate of 400Gb/s. Reversely, on the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 8 channels of 50Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the OSFP DR4+ module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.

The product is designed with form factor optical/electrical connection and digital diagnostic interface according the OSFP Multi-Source Agreement (MSA). It have been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Storage Temperature	*Ts*	-40		85	°C	
Operating Case Temperature	T_{op}	0		70	°C	
Power Supply Voltage	V_{cc}	-0.5		3.6	V	
Relative Humidity (non-condensation)	*RH*	0		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Operating Case Temperature	T_{op}	0		70	°C	
Power Supply Voltage	V_{cc}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		Gb/s	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	*D*	0.5		500	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Diagnostics Monitoring

Parameter	Symbol	Accuracy	Unit	Notes
Temperature monitor absolute error	DMI_Temp	± 3	°C	Over operating Temp
Supply voltage monitor absolute error	DMI_VCC	± 0.1	V	Full operating range
RX power monitor absolute error	DMI_RX	± 2 dB	dBm	1
Bias Current monitor	DMI_Bias	± 10%	mA	
Laser power monitor absolute error	DMI_TX	± 2 dB	dBm	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Transmitter						
Date Rate, each Lane			53.125 ± 100 ppm		Gb/s	
Modulation Format			PAM4			
Side-mode Suppression Ratio	*SMSR*	30			dB	Modulated
Center Wavelength		1304.5	1310	1317.5	nm	
Average Launch Power, each Lane	P_{AVG}	-2.4		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-0.2		4.2	dBm	2
Launch Power in OMA_{outer} mimus TDECQ, each Lane		-1.6 -1.5			dB	ER≥4.5 ER≥4.5
Transmitter and Dispersion Eye Closure for PAM4, each lane	*TDECQ*			3.4	dB	
Extinction Ration	*ER*	3.5			dB	
$RIN_{17.1}$ OMA	*RIN*			-136	dB/Hz	
Optical Return Loss Tolerance	*TOL*			17.1	dB	
Transmitter Reflectance	T_R			-26	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-15	dBm	
Receiver						
Data Rate, each Lane			53.125 ± 100 ppm		Gb/s	
Modulation Format			PAM4			
Damage Threshold, each Lane	TH_4	5.5			dBm	3
Average Receiver Power, each Lane		-6.4		4.5	dBm	4
Receiver Power (OMA_{outer}), each Lane				4.7	dBm	
Receiver sensitivity (OMA_{outer}), each lane	*SEN*			-4.5	dBm	5
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	*SRS*			-2.5	dBm	6
Receiver Reflectance	R_R			-26	dB	

LOS Assert	*LOSA*	-30		dBm
LOS De-assert	*LOSD*		-12	dBm
LOS Hysteresis	*LOSH*	0.5		dB
Stressed Conditions for Stress Receiver Sensitivity (Note 7)				
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4	dB
OMA_{outer} of each Aggressor Lane			4.2	dBm

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant, however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4dB, the OMA_{outer} (min) must exceed the minimum value specified here.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Average receiver power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant, however, a value above this does not ensure compliance.
5. Receive sensitivity ($OMA_{outer)}$, each lane (max) is informative and is defined for a transmitter with SECQ of 0.9dB.
6. Measured with conformance test signal for BER=2.4x10-4. A compliant receiver shall have stressed receiver sensitivity ($OMA_{outer)}$ value below the mask of Figure 5, for SECQ values between 0.9 and 3.4dB.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Electronical Characteristics

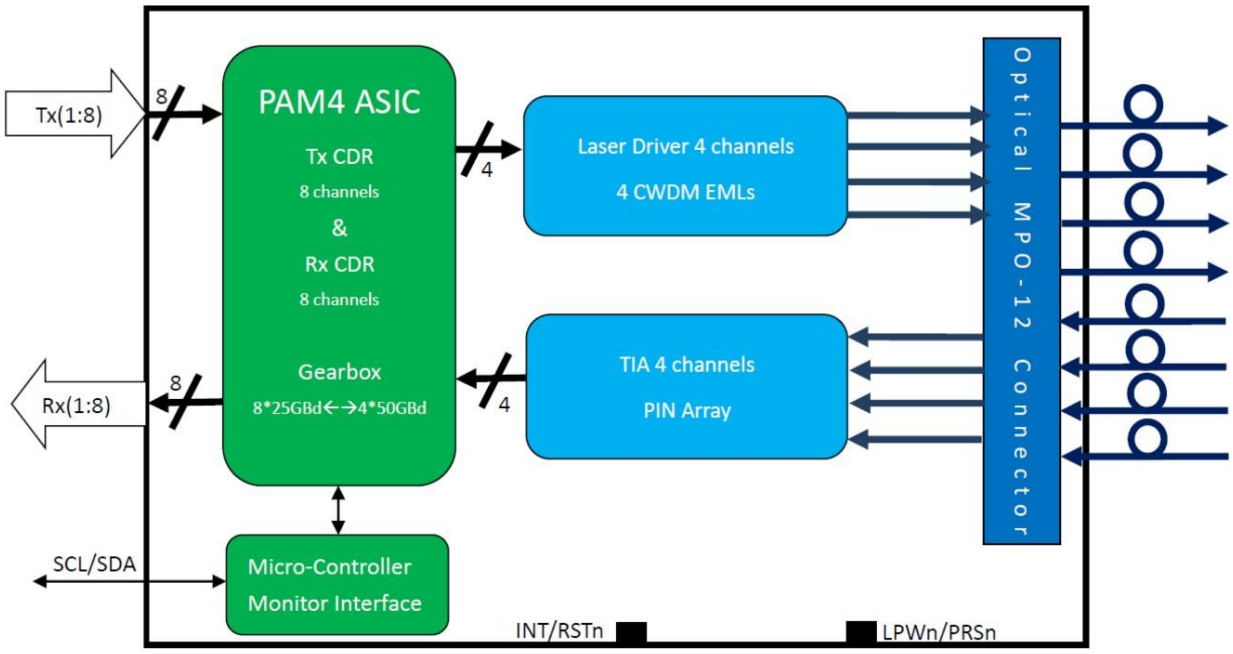
Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Power Consumption				12	W	
Supply Current	*Icc*			3.64	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	*TP1*		26.5625 ± 100 ppm		Gb/s	
Differential pk-pk Input Voltage Tolerance	*TP1a*	900			mVpp	1
Differential Termination Mismatch	*TP1*			10	%	
Differential Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	*TP1a*		See IEEE 802.3bs 120E.3.4.1			2
Single-ended Voltage Tolerance Range (Min)	*TP1a*		-0.4 to 3.3		V	
DC Common Mode Input Voltage	*TP1*	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each lane	*TP4*		26.5625 ± 100 ppm		Gb/s	
Differential Peak-to-Peak Output Voltage	*TP4*			900	mVpp	
AC Common Mode Output Voltage, RMS	*TP4*			17.5	mV	
Differential Termination Mismatch	*TP4*			10	%	
Differential Output Return Loss	*TP4*	IEEE 802.3-2015 Equation (83E-2)				

Common to Differential Mode Conversion Return Loss	*TP4*	IEEE 802.3-2015 Equation (83E-3)			
Transition Time 20% to 80%	*TP4*	9.5		Ps	
Near-end Eye Symmetry Mask Width (ESMW)	*TP4*		0.265	UI	
Near-end Eye Height, Differential	*TP4*	70		mV	
Far-end Eye Symmetry Mask Width (ESMW)	*TP4*		0.2	UI	
Far-end Eye Height, Differential	*TP4*	30		mV	
Far-end Pre0cursor ISI Ratio	*TP4*	-4.5	2.5	%	
Common Mode Output Voltage (Vcm)	*TP4*	-350	2850	mV	3

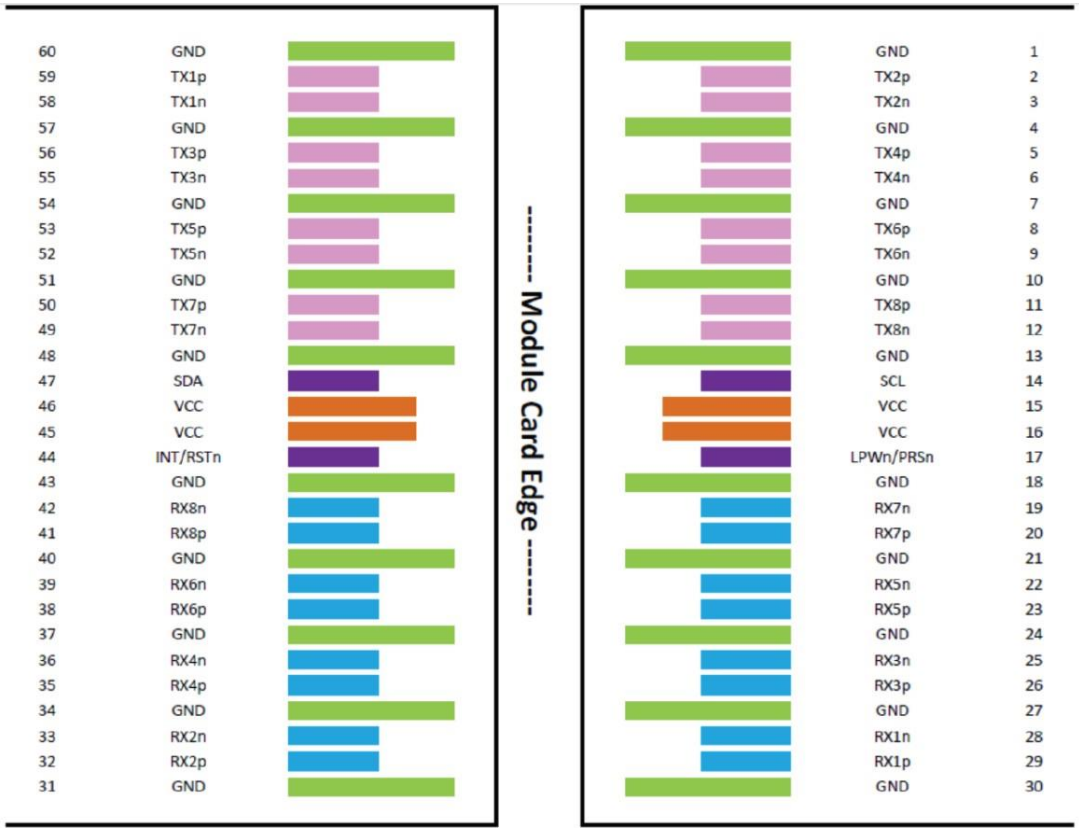
Notes:

1. With the exception to IEEE 802.3bs 120E3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E 1.1.
3. DC common mode voltage generated by the host Specification includes effects of ground offset voltage.

Transceiver Block Diagram



Pin Assignment and Description



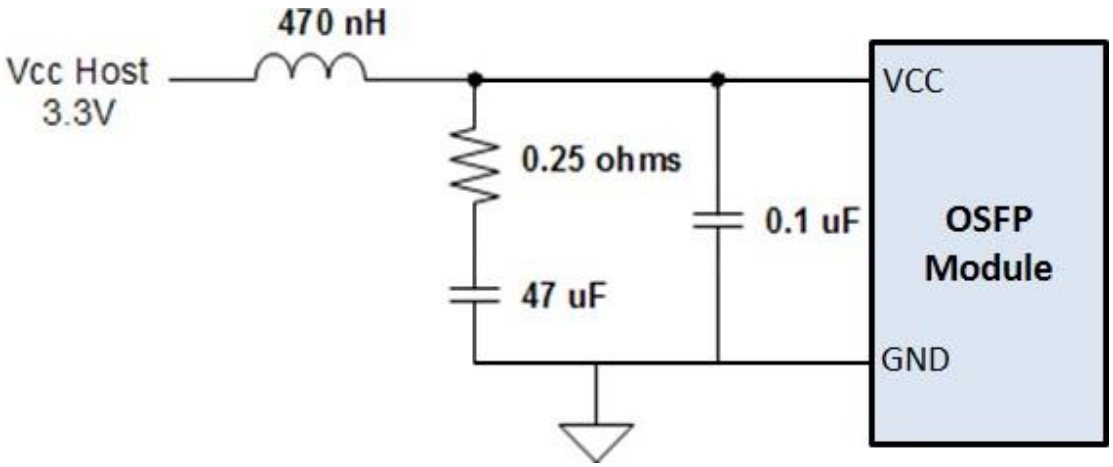
Pin Descriptions

Pin	Symbol	Description	Logic	Description	Note
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Hos	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Hos	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Hos	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Hos	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	KVCNIS I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present		Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3

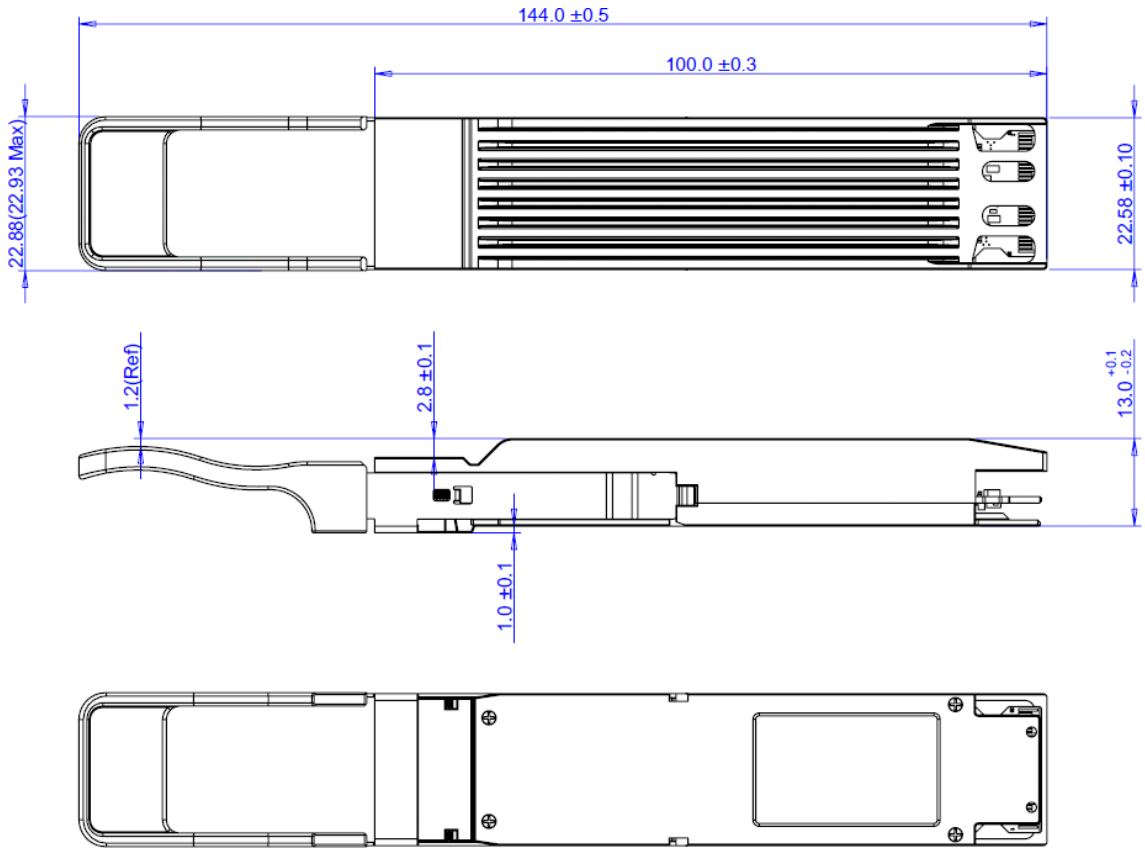
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Non-Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Non-Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Non-Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Non-Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3

60	GND		Ground		

Recommended Power Supply Filter



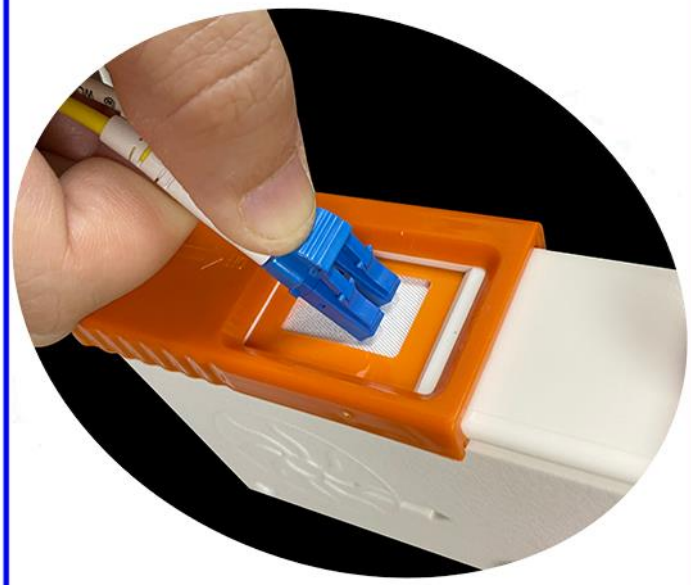
Dimensions


144.0 ±0.5
100.0 ±0.3
22.88(22.93 Max)
22.58 ±0.10
1.2(Ref)
2.8 ±0.1
13.0 +0.1 -0.2
1.0 ±0.1

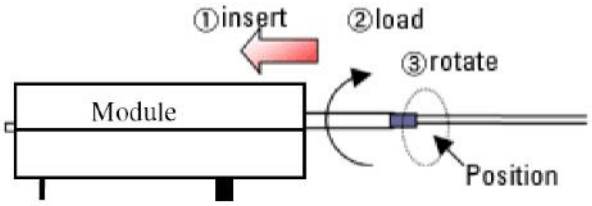
Optical Receptacle Cleaning Recommendations :

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.

Cleaning of patch-cord



Cleaning of fiber stub



1. Insert
   Ensure that stick is held straight when inserting into sleeve.
2. Load
   Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve.
3. Rotate
   Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained.

Notice: Number of possible wipes:
Maintenance (repair) ~1 use / piece
Equipment construction: 4 uses / piece (max.)

Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information

Model Number	Part Number	Voltage	Temperature
400G OSFP DR4-2km	OPOY-S02-13-CBS	3.3V	0°C to 70 °C

Modification History

Revision	Date	Description
A1	Apr. 2019	Initial Release

Note: All information contained in this document is subject to change without notice.