Features

- QSFP-DD MSA compliant
- Parallel 4 Optical Lanes
- 100G Lambda MSA 100G-FR Specification compliant
- Up to 2km transmission on single mode fiber (SMF) with FEC
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel
- Maximum power consumption 8.5W
- MPO-12 connector
- Operating case temperature: 0°C ~70°C
- RoHS compliant

Applications

- 400G Ethernet
- Infiniband interconnects
- Datacenter Enterprise networking

Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s. Reversely, on the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rage of 400Gb/s into 8 channels of 50Gb/s (PAM4) electrical output data.

An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP-DD DR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP-DD MSA-compliant edge type connector.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Mulit-Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	*Tst*	-40	85	°C	
Supply Voltage	Vcc	-0.5	3.6	V	
Case Operating Temperature	T_{op}	0	70	°C	
Humidity (non-condensing)	*Rh*	0	85	%	
Damage Threshold, each Lane	*THd*	5		dBm	
Data Input Voltage Differential pk-pk	*Vpp*	100	900	mV	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Operating Case Temperature	*Tca*	0		70	°C	
Supply Voltage	V_{cc}	3.135	3.3	3.465	V	
Electrical Data Rage, each Lane			26.5625		GBd	PAM4
Optical Data Rage, each Lane			53.125		GBd	PAM4
Power Supply Noise	*Vn*			66	mV	
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$24x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-15}$		1
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance	*D*	0.002		2		2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum transmission distance.

Diagnostic Monitoring Interface

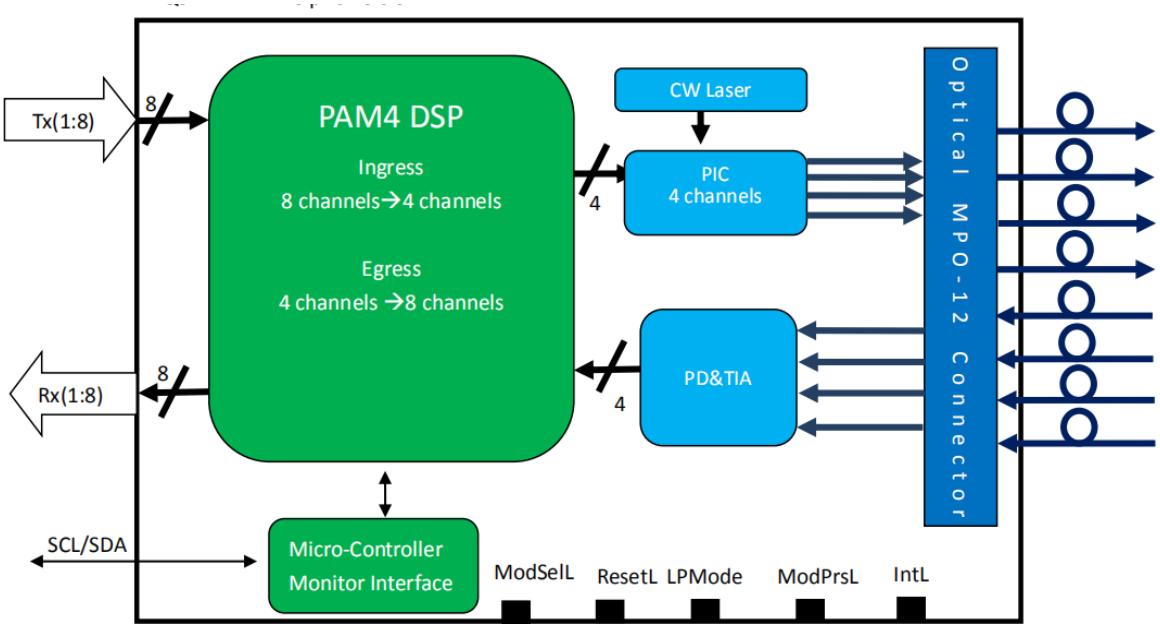
Parameter	Symbol	Accuracy	Unit	Notes
Temperature monitor absolute error	DMI_Temp	± 3	°C	Over operating
Supply voltage monitor absolute error	DMI_VCC	± 0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	± 3	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	± 10%	mA	

Channel TX power monitor absolute error	DMI_TX_Ch	± 3	dB	1

Notes:

1.Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/-3 dB total accuracy.

Transceiver Block Diagram



Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Signaling Rate, each Lane	*DR*		53.125 ± 100ppm		GBd	PAM4
Center Wavelength	λc	1304.5	1310	1317.5	NM	
			Transmitter			
Side-mode Suppression Ratio	*SMSR*	30			dB	
Average Launch Power, each Lane	P_{AVG}	-2.4		4	dBm	1
Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-0.2		4.2	dBm	2
Launch Power in OMA_{outer} minus TDECQ, each lane		-1.6			dB	For ER≧ 4.5dB
		-1.5			dB	For ER≦ 4.5dB
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), each lane	*TDECQ*			3.4	dB	SSPRQ
TDECQ-10*$\log_{10}(C_{eq})$,each Lane				3.4	dB	3
Extinction Ratio	*ER*	3.5			dB	
$RIN_{21.4}$ OMA	*RIN*			-136	dB/Hz	
Optical Return Loss Tolerance	*TOL*			17.1	dB	
Transmitter Reflectance	R_T			-26	dB	
Average Launch Power of OFF Transmitter, each Lane	*Poff*			-15	dBm	
LOS Assert Level	*LOSA*		50		mV	4
LOA De-assert Level	*LOSD*		100		mV	
			Receiver			
Damage Threshold, each Lane	*THd*	5			dBm	5
Average receiver Power, each Lane		-6.4		4	dBm	6
Receiver Power (OMA_{outer}), each Lane				4.2	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	*SEN*			Equation (1)	dBm	7
Stressed Receiver Sensitivity in OMA_{outer}, each Lane	*SRS*			-2.	dBm	8
BER @RxAOP= -2dBm				$2x10^{-6}$		9
BER @RxAOP= -0dBm				$2x10^{-6}$		9
BER @RxAOP= +2dBm				$2x10^{-6}$		9

BER @RxAOP= +4.5dBm			$2x10^{-5}$		9
Receiver Reflectance	R_R		-26	dB	
LOS Assert	*LOSA*	-15	-11	dBm	10
LOS De-assert	*LOSD*	-14	-10	dBm	
LOS Hysteresis	*LOSH*	0.5	5	dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 11)					
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		3.4		dB	
SECQ-10*$\log_{10}(C_{eq})$, Lane under test			3.4	dB	
OMA_{outer} of each Aggressor Lane		4.2		dBm	

Notes:

1 · Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant, however, a value above this does not ensure compliant. Average launch power is tested with PRBS31Q.

2 · Even if the TDECQ < 1.4dB fo ran extinction ratio of ≧4.5dB or TDECQ < 1.3dB for an extinction ratio of < 4.5dB, the OMA_{outer} (min) must exceed the minimum value specified here. OMA_{outer} is tested with PRBS13Q.

3 · C_{eq} is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.

4 · When Tx LOS asserted, the Tx squelch will be triggered to shut OMA output

5 · The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operated correctly at this input power.

6 · Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliant Average receive power is tested with PRBS31Q.

7 · Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 0.9dB to 3.4dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 4. It is tested with PRBS31Q pattern at BER of $2.0x10^{-4}$

$$RS=\max(-4.5, SECQ-5.9)\ dBm \quad (1)$$

Where

RS is the receiver sensitivity,

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

8 · Measured with conformance test signal at TP3 for the BER equal to $2.0x10^{-4}$

9 · Measured with PRBS31Q pattern and the reference transmitter with a value of TDECQ up to 3.4dB

10 · Rx LOS is upon average input power. Rx Squelch will be triggered when Rx LOS is asserted.

11 · These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Electronical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Power Consumption				8.5	W	
Supply Current	*Icc*			2.58	A	
Power Supply Ripple				15	mv	
Transmitter (each Lane)						
Signaling Rate, each Lane	*TP1*		26.5625 ± 100 ppm		GBd	
Differential pk-pk Input voltage Tolerance	*TP1a*	900			mVpp	1
Differential Termination Mismatch	*TP1*			10	%	
Differential Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-5)			Db	
Differential to Common Mode Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-6)			Db	
Module Stressed Input Test	*TP1a*		See IEEE 802.3bs 120E.3.4.1			2
Single-ended Voltage Tolerance Range (Min)	*TP1a*		-0.4 to 3.3		V	
DC Common Mode Input Voltage	*TP1*	-350		2850	Mv	3
Input AC Coupling Capacitor	*TP1a*		0.1		uF	
Receiver (each Lane)						
Differential Peak to Peak output voltage	*TP4*			900	mVpp	
AC Common Mode Output Voltage, RMS	*TP4*			17.5	Mv	
Differential Termination Mismatch	*TP4*			10	%	
Differential Output Return Loss	*TP4*	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return	*TP4*	IEEE 802.3-2015 Equation				

		(83E-3)				
Transition Time, 20% to 80%	*TP4*	9.5			Ps	
Near-end Eye Symmetry Mask Width (ESMW)	*TP4*	0.265			UI	
Near-end Eye Height, Differential	*TP4*	70			Mv	
Far-end Eye Symmetry Mask Width (ESMW)	*TP4*	0.2			UI	
Far-end Eye Height, Differential	*TP4*	30			Mv	
Far-end Pre-cursor ISI Ratio	*TP4*	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	*TP4*	-350		2850	Mv	3
Output AC Coupling Capacitor	*TP4*		0.1		uf	

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Pin Assignment and Description

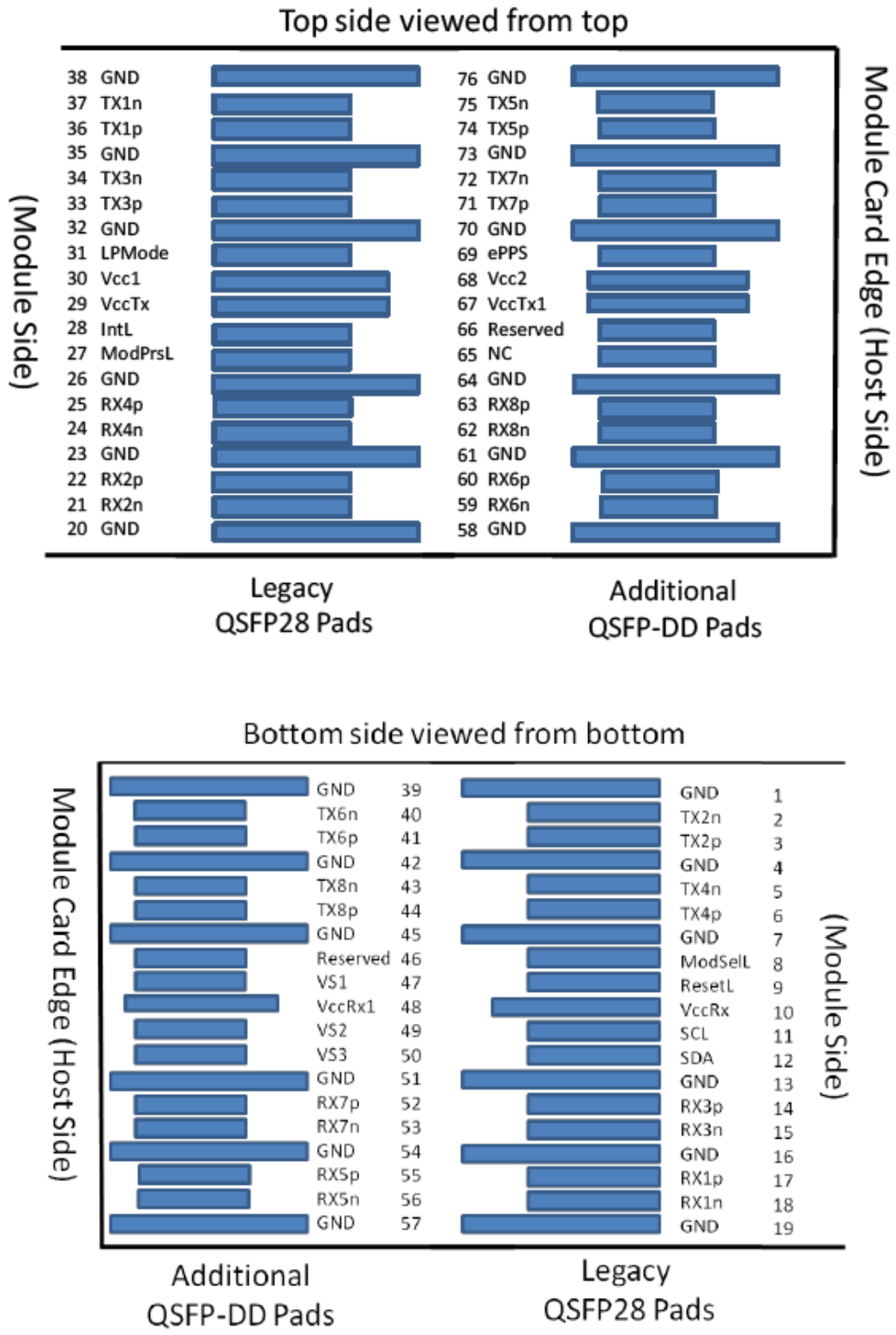


Figure2. Electrical Pin-out Details

Pin Descriptions

PIN	Logic	Symbol	Name / Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter inverted data input	
3	CML-I	Tx2p	Transmitter non-inverted data input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter inverted data input	
6	CML-I	Tx4p	Transmitter non-inverted data input	
7		GND	Ground	1
8	LVTTL-I	MoDSeIL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3v Receiver Power Supply	2
11	LVCMOS-I/O	SCL	2-wire Serial interface clock	
12	LVCMOS-I/O	SDA	2-wire Serial interface data	
13		GND	Ground	1
14	CML-O	RX3p	Receiver non-inverted Data Output	
15	CML-O	RX3n	Receiver inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver non-inverted Data Output	
18	CML-O	Rx1n	Receiver inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3v Power supply transmitter	2
30		Vcc1	+3.3v Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	

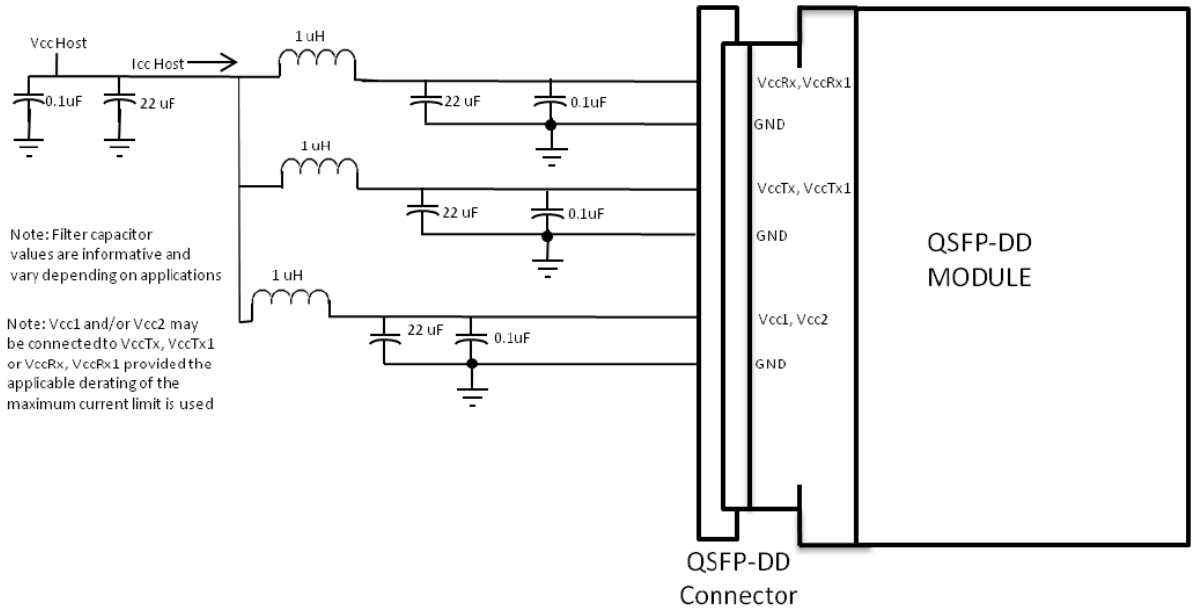
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	
47		VS1	Module Vendor Specific 1	
48		VccRx1	3.3V Power Supply	
49		VS2	Module Vendor Specific 2	
50		VS3	Module Vendor Specific 3	
51		GND	Ground	1
52	CML-O	Rx7p-	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p-	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n-	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For Future Use	3

70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

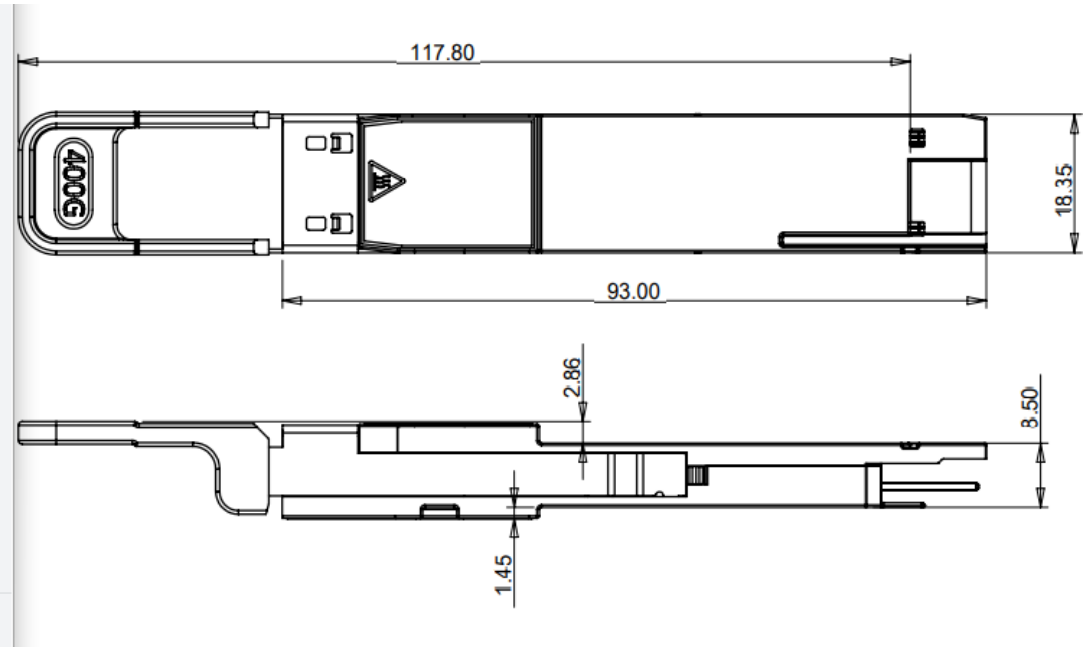
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, RccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vccl, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The corrector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved, No connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Recommended Power Supply Filter



Host Board Power Supply Filtering

Dimensions

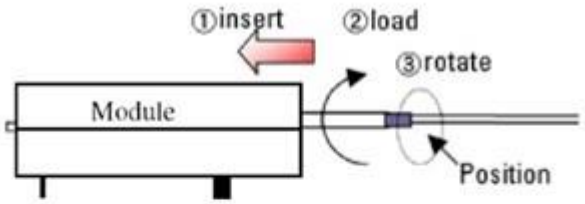


Optical Receptacle Cleaning Recommendations :

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.

Cleaning of patch-cord

Cleaning of fiber stub



1. Insert
   Ensure that stick is held straight when inserting into sleeve.
2. Load
   Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve.
3. Rotate
   Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained.

Notice: Number of possible wipes:
Maintenance (repair) ~1 use / piece
Equipment construction: 4 uses / piece (max.)

Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information

Model Number	Part Number	Reach	Wavelength	Temperature
QSFP-DD 400G DR4+	OPDY-S02-13-CBS	2km	1310nm	0°C to 70°C

Modification History

Revision	Date	Description
A1	Sep. 2021	Initial Release

Note: All information contained in this document is subject to change without notice.