Features

- QSFP-DD MSA compliant
- Up to 100m OM4, 70m OM3 MMF transmission
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel
- Maximum power consumption 12W
- MPO-12 connector
- Single 3.3V power supply
- Operating case temperature: 0℃ ~70℃
- RoHS-6 compliant

Applications

- Data Center
- Infiniband HDR, EDR

Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) Bi-Direction optical module . The module accepts eight host electrical data and transmits them in two groups of optical bi-directional lanes (each group contains 4 pairs of optical lane) to allow optical communication over optical multi-mode fibers. Reversely, on the receiver side, the module accepts 8 sets of optical input signal and converts them to 8 channels of electrical data.

An optical fiber with an MPO-12 connector can be plugged into the QSFP-DD module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an MSA-compliant 76-pin edge type connector.

The module operates by a single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receiver more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA). It has designed to meet the harshest external operating conditions including temperature, humidity, and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	*Tst*	-40	85	°C	
Supply Voltage	Vcc	-0.5	3.6	V	
Case Operating Temperature	T_{op}	0	70	°C	
Humidity (non-condensing)	*Rh*	0	85	%	
Damage Threshold, each Lane	*THd*	3.4		dBm	

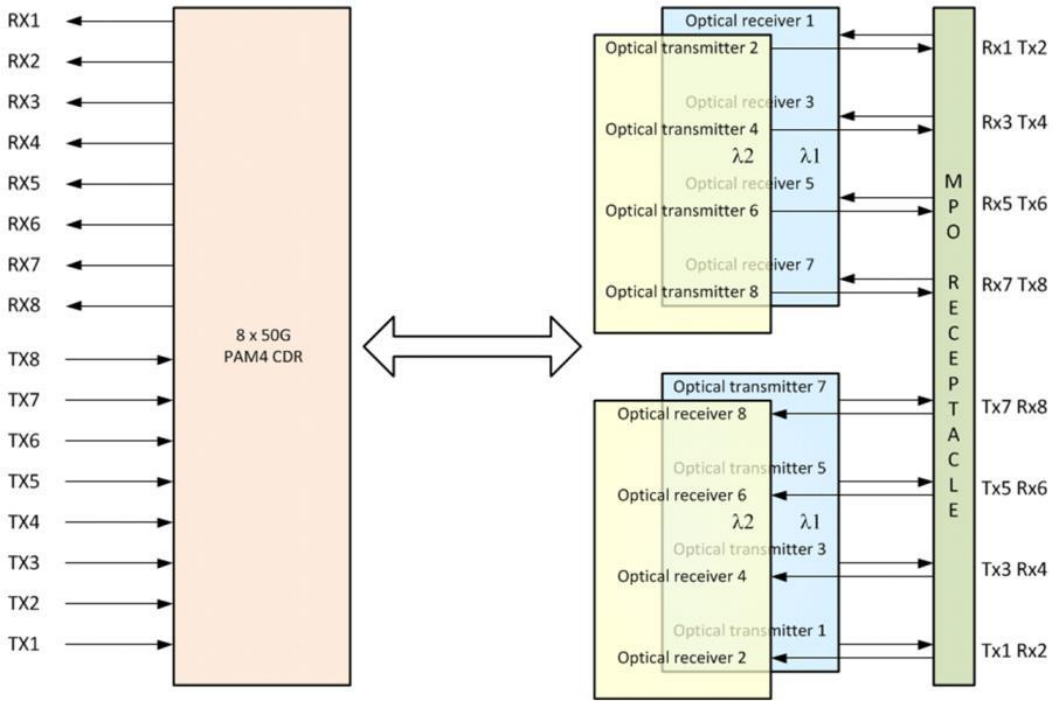
Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Operating Case Temperature	*Tca*	0		70	°C	
Supply Voltage	V_{cc}	3.135	3.3	3.465	V	
Data Rate, each Lane	*fd*		26.5625		GBd	
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Prost-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance with OM3	*D*	0.5		70	M	2
Link Distance with OM4	*D*	0.5		100	M	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Transceiver Block Diagram



Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Center Wavelength	$\lambda 1$	844		863	nm	
	$\lambda 2$	900		918	nm	
Transmitter						
RMS Spectral Width	$\Delta \lambda rms$			$\lambda 1$: 0.6 $\lambda 2$: 0.65	nm	
Average Launch Power, each Lane	P_{AVG}	-6.5		4	dBm	1
Optical Modulation Amplitude (OMA), each Lane	P_{OMA}	-4.5		3	dBm	2
Launch Power in OMA minus TDECQ, each Lane		-5.9			dB	
Transmitter Dispersion Penalty, each Lane	*TDECQ*			4.5	dB	3
TDECQ-10*log10(C_{eg}), each Lane				4.5		4
Extinction Ratio	*ER*	3.0			dB	
RIN_{12} OMA	*RIN*			-128	dB/Hz	
Optical Return Loss Tolerance	*TOL*	12			dB	
Average Launch Power of OFF Transmitter, each Lane	*Poff*			-30	dBm	
Encircled Flux			≧86% at 19μm ≦30% at 4.5μm			5
Receiver						
Signaling rate, each Lane			26.5625 ± 100ppm		Gbps	
Damage Threshold, each Lane	*THd*	5			dBm	6
Average receiver Power, each Lane		-8.5		4	dBm	7
Receiver Power (OMA), each Lane				3.0	dBm	
Receiver Sensitivity (OMA), each Lane	*SEN*			Max (-6.6, SECQ-8) Refer to Figure 5	dBm	9
Receiver Reflectance	R_R			-12	dB	
Stressed receiver sensitivity in OMA, each Lane				-3.5	dBm	8

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant, however, a value above this does not ensure compliant.
2. Even if the TDECQ < 1.4dB , the OMA_{outer} (min) must exceed this value.
3. TDECQ is specified and measured as per IEEE802.3cm Clause 150.8.5.
4. C_{eq} is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.8 which accounts for reference equalizer noise enhancement.
5. If measured into type A1a.2, or type A1a.3, or type A1a4, 50 um fibers in accordance with IEC 61280-1-4.
6. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
7. Average receiver power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
8. Measured with a conformance test signal at TP3 (see IEEE 802.3 CI 150) for the BER specified. They are not characteristics of the receiver. The conditions for measuring stressed receiver sensitivity are the following:

Stressed eye closure (SECQ), lane under test	.5	B
ECQ – 10log10(Ceq) lane under test (max)	.5	Bm
)MAouter of each aggressor lane	.0	Bm

9. Receiver sensitivity is considered a normative requirement. RX sensitivity is defined for a transmitter with a value of SECQ up to 4.5dB. For transmitter with SECQ different from 4.5dB, limit is reported as per figure 5

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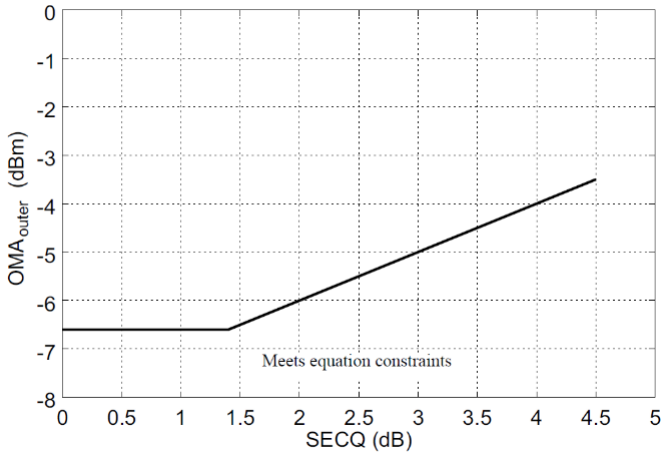


Electronical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Power Consumption				12	W	
Supply Current	*Icc*			3.63	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	*TP1*		26.5625 ± 100 ppm		GBd	
Differential pk-pk Input voltage Tolerance	*TP1a*	900			mVpp	1
Differential Termination Mismatch	*TP1*			10	%	
Differential Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-5)			Db	
Differential to Common Mode Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-6)			Db	
Module Stressed Input Test	*TP1a*	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	*TP1a*		-0.4 to 3.3		V	
DC Common Mode Input Voltage	*TP1*	-350		2850	Mv	3
Input AC Coupling Capacitor	*TP1a*		0.1		uF	
Receiver (each Lane)						
Differential Peak to Peak output voltage	*TP4*			900	mVpp	
AC Common Mode Output Voltage, RMS	*TP4*			17.5	Mv	
Differential Termination Mismatch	*TP4*			10	%	
Differential Output Return Loss	*TP4*	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return	*TP4*	IEEE 802.3-2015 Equation (83E-3)				

Transition Time, 20% to 80%	*TP4*	9.5		Ps	
Near-end Eye Symmetry Mask Width (ESMW)	*TP4*		0.265	UI	
Near-end Eye Height, Differential	*TP4*	70		Mv	
Far-end Eye Symmetry Mask Width (ESMW)	*TP4*		0.2	UI	
Far-end Eye Height, Differential	*TP4*	30		Mv	
Common Mode Output Voltage (Vcm)	*TP4*	-4.5	2.5	%	
Common Mode Output Voltage (Vcm)	*TP4*	-350	2850	Mv	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Pin Assignment and Description

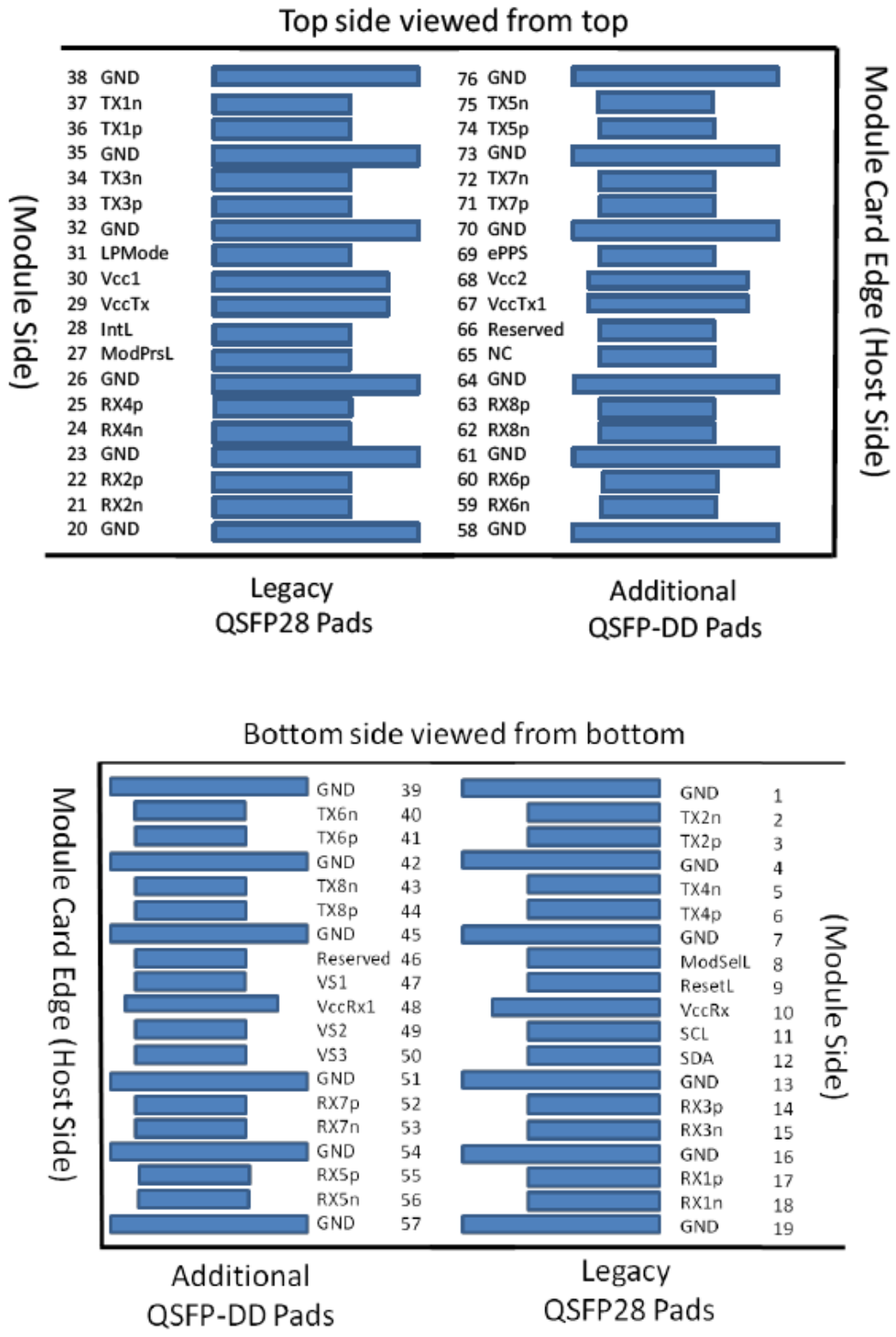


Figure2. Electrical Pin-out Details

Pin Descriptions

PIN	Logic	Symbol	Name / Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter inverted data input	
3	CML-I	Tx2p	Transmitter non-inverted data input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter inverted data input	
6	CML-I	Tx4p	Transmitter non-inverted data input	
7		GND	Ground	1
8	LVTTL-I	MoDSeIL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3v Receiver Power Supply	2
11	LVCMOS-I/O	SCL	2-wire Serial interface clock	
12	LVCMOS-I/O	SDA	2-wire Serial interface data	
13		GND	Ground	1
14	CML-O	RX3p	Receiver non-inverted Data Output	
15	CML-O	RX3n	Receiver inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver non-inverted Data Output	
18	CML-O	Rx1n	Receiver inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3v Power supply transmitter	2
30		Vcc1	+3.3v Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	

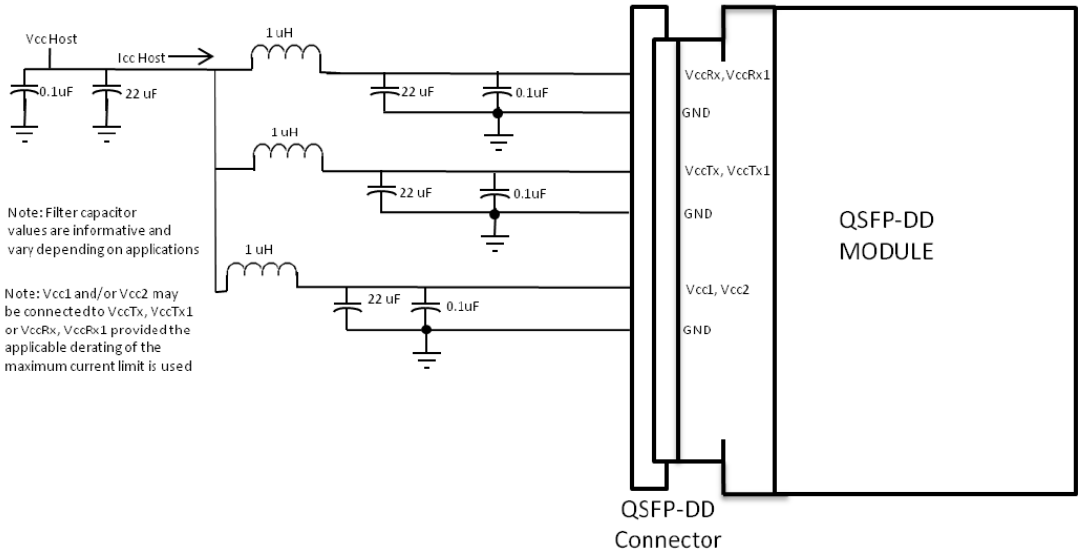
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	
47		VS1	Module Vendor Specific 1	
48		VccRx1	3.3V Power Supply	
49		VS2	Module Vendor Specific 2	
50		VS3	Module Vendor Specific 3	
51		GND	Ground	1
52	CML-O	Rx7p-	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p-	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n-	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For Future Use	3

70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

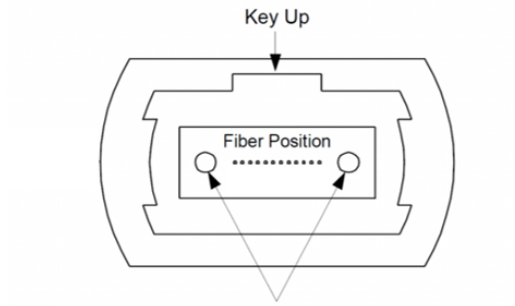
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, RccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vccl, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The corrector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved, No connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

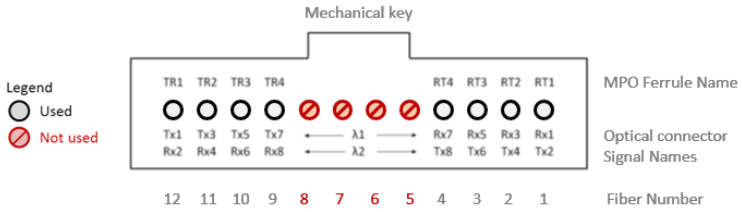
Recommended Power Supply Filter



Host Board Power Supply Filtering

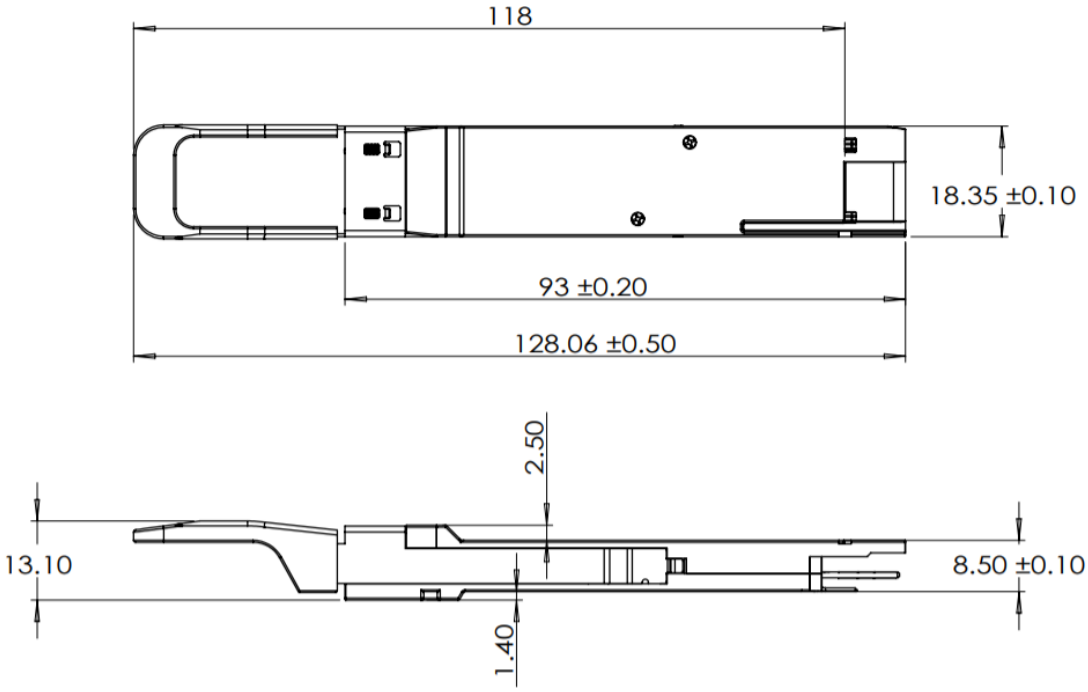


2 Alignent PIN are present
The Central Four fibers may be physically present



Outside View of the QSFPDD MPO-12 Receptacle

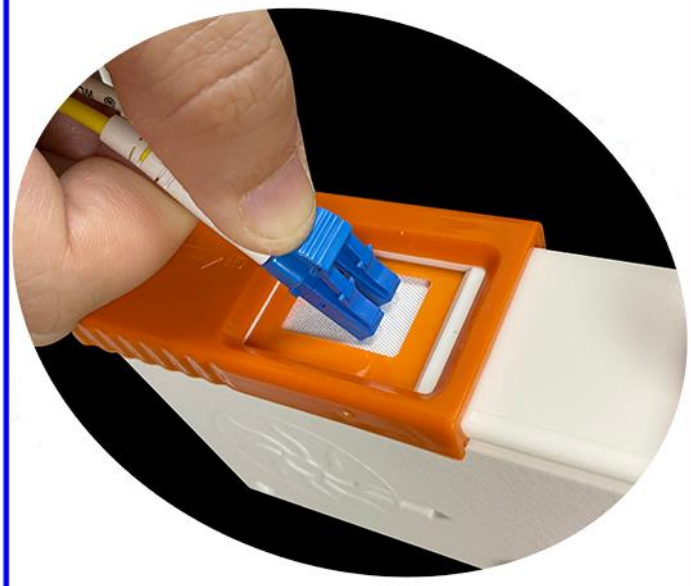
Dimensions



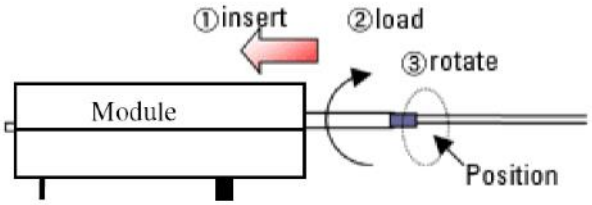
Optical Receptacle Cleaning Recommendations :

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.

Cleaning of patch-cord



Cleaning of fiber stub



1. Insert
   Ensure that stick is held straight when inserting into sleeve.
2. Load
   Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve.
3. Rotate
   Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained.

Notice: Number of possible wipes:
Maintenance (repair) ~1 use / piece
Equipment construction: 4 uses / piece (max.)

Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information

Model Number	Part Number	Reach	Wavelength	Temperature
QSFP-DD 400G BiDi SR4	OPDY-WX1-85-CB	100m	850nm	0°C to 70°C

Modification History

Revision	Date	Description
A1	Aug. 2020	Initial Release

Note: All information contained in this document is subject to change without notice.