



Features

- QSFP-DD MSA compliant
- 8 parallel lanes on 850nm center wavelength
- Compliant to IEEE 802.3bs Specification
- Up to 70m transmission on multi-mode fiber (MMF) OM3 with FEC
- Operating case temperature: 20 to 60oC
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 53.125Gbps (PAM4) per channel.
- Maximum power consumption 10W
- MPO-16 connector
- RoHS compliant

Applications

- Data Center Interconnect
- 400G Ethernet
- Infiniband interconnects
- Enterprise networking

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units | Note |
|--------------------------------------|----------|------|------|-------|------|
| Storage Temperature | T_s | -40 | 85 | °C | |
| Operating Case Temperature | T_{op} | 20 | 60 | °C | |
| Power Supply Voltage | V_{cc} | -0.5 | 3.6 | V | |
| Relative Humidity (non-condensation) | RH | 0 | 85 | % | |

Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units | Note |
|--------------------------|----------|-------|---------|----------------------|-------|------|
| Operating Temperature | T_{op} | 20 | | 60 | °C | |
| Power Supply Voltage | V_{cc} | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 26.5625 | | GBd | PAM4 |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Pre-FEC Bit Error Ratio | | | | 2.4×10^{-4} | | |
| Post-FEC Bit Error Ratio | | | | 1×10^{-12} | | 1 |
| Link Distance (OM3 MMF) | D | 0.5 | | 70 | m | 2 |

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Diagnostics Monitoring

| Parameter | Symbol | Accuracy | Unit | Notes |
|---|--------------|------------|------|----------------------------------|
| Temperature monitor absolute error | DMI_Temp | ± 3 | °C | Over operating temperature range |
| Supply voltage monitor absolute error | DMI_VCC | ± 0.1 | V | Over full operating range |
| Channel RX power monitor absolute error | DMI_RX_Ch | ± 2 | dB | 1 |
| Channel Bias current monitor | DMI_Ibias_Ch | $\pm 10\%$ | mA | |
| Channel TX power monitor absolute error | DMI_TX_Ch | ± 2 | dB | 1 |

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/- 1 dB fluctuation, or a +/- 3 dB total accuracy.

Transmitter Electro-Optical Characteristics (each Lane)

| Parameter | Test Point | Min | Typ. | Max | Units | Notes |
|---|------------------------|----------------------------------|---------------------------------|------|-------|-----------|
| Power Consumption | | | | 10 | W | |
| Supply Current | <i>I_{cc}</i> | | | 3.03 | A | |
| Signaling Rate, each Lane | <i>TP1</i> | 26.5625 ± 100 ppm | | | GBd | |
| Differential pk-pk Input Voltage Tolerance | <i>TP1a</i> | 900 | | | mVpp | 1 |
| Differential Termination Mismatch | <i>TP1</i> | | | 10 | % | |
| Differential Input Return Loss | <i>TP1</i> | IEEE 802.3-2015 Equation (83E-5) | | | dB | |
| Differential to Common Mode Input Return Loss | <i>TP1</i> | IEEE 802.3-2015 Equation (83E-6) | | | dB | |
| Module Stressed Input Test | <i>TP1a</i> | See IEEE 802.3bs 120E.3.4.1 | | | | 2 |
| Single-ended Voltage Tolerance Range (Min) | <i>TP1a</i> | | -0.4 to 3.3 | | V | |
| DC Common Mode Input Voltage | <i>TP1</i> | -350 | | 2850 | mV | 3 |
| Center Wavelength | λ_c | 840 | 850 | 860 | nm | |
| Data Rate, each Lane | | 26.5625 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| RMS Spectral Width | $\Delta\lambda_{rms}$ | | | 0.6 | nm | Modulated |
| Average Launch Power, each Lane | <i>P_{AVG}</i> | -6 | | 4 | dBm | 4 |
| Outer Optical Modulation Amplitude (OMA _{outer}), each Lane | <i>P_{OMA}</i> | -4 | | 3 | dBm | 5 |
| Launch Power in OMA _{outer} minus TDECQ, each Lane | <i>TDECQ</i> | | | 4 | dB | |
| Extinction Ratio | <i>ER</i> | 3 | | | dB | |
| Optical Return Loss Tolerance | <i>TOL</i> | | | 12 | dB | |
| Average Launch Power OFF Transmitter, each Lane | <i>P_{off}</i> | | | -30 | dBm | |
| Encircled Flux | | | ≥ 86% at 19μm ≥ 30% at 4.5μm | | | |

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
4. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Even if the TDECQ < 1 dB , the OMAouter (min) must exceed the minimum value specified here.



Receiver Electro-Optical Characteristics (each Lane)

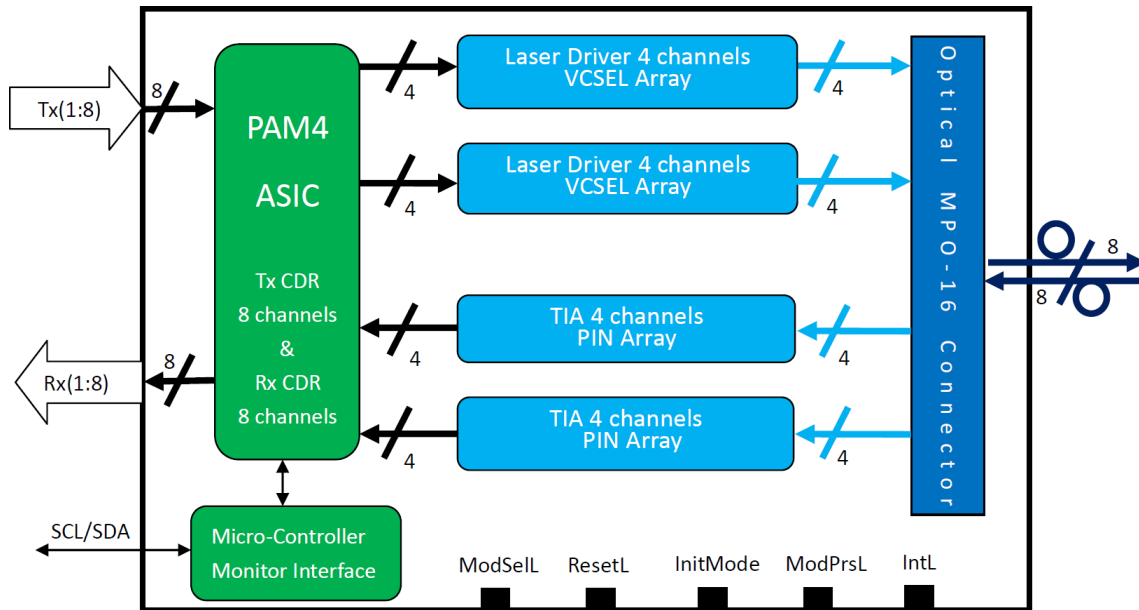
| Parameter | Test Point | Min | Typ. | Max | Units | Notes |
|--|------------|-------------------|-------|----------------------------------|-------|-------|
| Signaling Rate, each lane | TP4 | 26.5625 ± 100 ppm | | | GBd | |
| Differential Peak-to-Peak Output Voltage | TP4 | | | 900 | mVpp | |
| AC Common Mode Output Voltage, RMS | TP4 | | | 17.5 | mV | |
| Differential Termination Mismatch | TP4 | | | 10 | % | |
| Differential Output Return Loss | TP4 | | | IEEE 802.3-2015 Equation (83E-2) | | |
| Common to Differential Mode Conversion Return Loss | TP4 | | | IEEE 802.3-2015 Equation (83E-3) | | |
| Transition Time, 20% to 80% | TP4 | 9.5 | | | ps | |
| Near-end Eye Symmetry Mask Width (ESMW) | TP4 | | 0.265 | | UI | |
| Near-end Eye Height, Differential | TP4 | 70 | | | mV | |
| Far-end Eye Symmetry Mask Width (ESMW) | TP4 | | 0.2 | | UI | |
| Far-end Eye Height, Differential | TP4 | 30 | | | mV | |
| Far-end Pre-cursor ISI Ratio | TP4 | -4.5 | | 2.5 | % | |
| Common Mode Output Voltage (V _{cm}) | TP4 | -350 | | 2850 | mV | 1 |
| Center Wavelength | Ac | 840 | 850 | 860 | nm | |
| Data Rate, each Lane | | 26.5625 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Damage Threshold, each Lane | THd | 5 | | | dBm | 2 |
| Average Receive Power, each Lane | | -7.9 | | 4 | dBm | 3 |
| Receive Power (OMA _{outer}), each Lane | | | | 3 | dBm | |
| Receiver Sensitivity (OMA _{outer}), each Lane | SEN | | | -7 | dBm | 4 |
| Stressed Receiver Sensitivity (OMA _{outer}), each Lane | SRS | | | -3 | dBm | 5 |

| Parameter | Test Point | Min | Typ. | Max | Units | Notes |
|---|------------|-----|------|-----|-------|-------|
| Receiver Reflectance | R_R | | | -12 | dB | |
| LOS Assert | LOSA | -30 | | | dBm | |
| LOS De-assert | LOSD | | | -12 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| Stressed Conditions for Stress Receiver Sensitivity (Note 6) | | | | | | |
| Stressed Eye Closure for PAM4 (SECQ), Lane under Test | | | 4 | | dB | |
| OMAouter of each Aggressor Lane | | | 3 | | dBm | |

Notes:

1. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
2. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. Receiver Sensitivity OMAouter, each lane (max) is informative and is defined for a BER of 2.4×10^{-4} .
5. Measured with conformance test signal at receiver input for the BER of 2.4×10^{-4} .
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Block Diagram of Transceiver



This product is a parallel 400Gb/s Quad Small Form Factor Pluggable--double density (QSFP-DD) optical module. It provides increased port density and total system cost savings. The QSFP-DD full- duplex optical module offers 8 independent transmit and receive channels, each capable of 53.125Gb/s operation for an aggregate data rate of 400Gb/s on 100 meters of OM3 multi-mode fiber.

An optical fiber cable with an MTP/MPO-16 connector can be plugged into the QSFP-DD SR8 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an QSFP-DD MSA-compliant edge type connector.

The central wavelengths of all the 8 parallel lanes are 850nm. It contains an optical MPO-16 connector for the optical interface and a 60-pin connector for the electrical interface. Host FEC is required to support up to 70m OM3 multi-mode fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

The module incorporates 8 parallel channels, on 850nm Center Wavelength, operating at 50G per channel. The transmitter path incorporates an 8-channel CDR retimer, 2 sets of quad channel VCSEL drivers together with 2 sets of VCSEL arrays. On the receiver path, 2 sets of photodiode arrays optics are coupled with an 8-channel CDR retimer. The electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA in the transmitting and receiving directions, and the optical interface is compliant to QSFP-DD MSA with MPO-16 Optical Connector. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. All the power supply pins are internally connected and should be applied concurrently. As per MSA specifications the module offers seven low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, InitMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2- wire serial communication commands. The ModSelL allows the use of this product on a single 2- wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Initialize Mode (InitMode) is an input signal. It is pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP28 module must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.

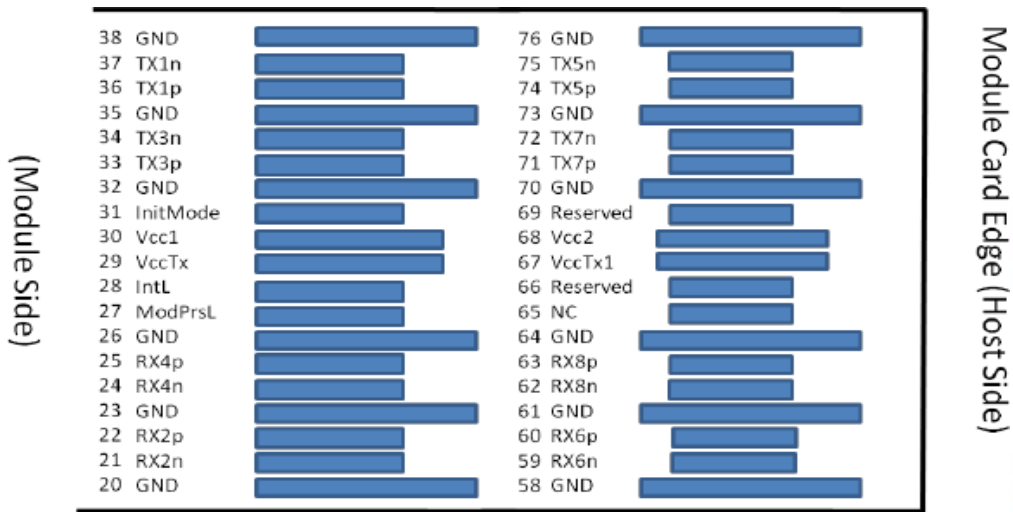
The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

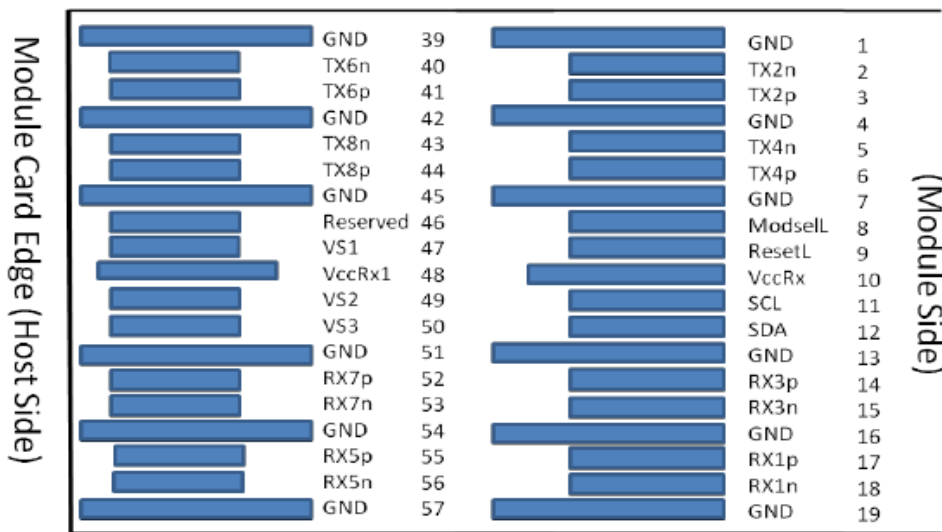
Optical interface and Pin Assignment



Top side viewed from top

Legacy QSFP28 Pads

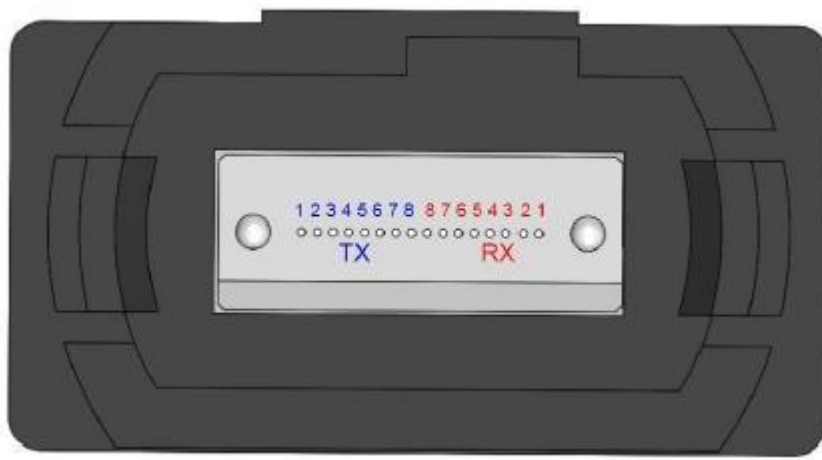
Additional QSFP-DD Pads



Bottom side viewed from bottom

Additional QSFP-DD Pads

Legacy QSFP28 Pads



MPO-16 Optical Connector Interface

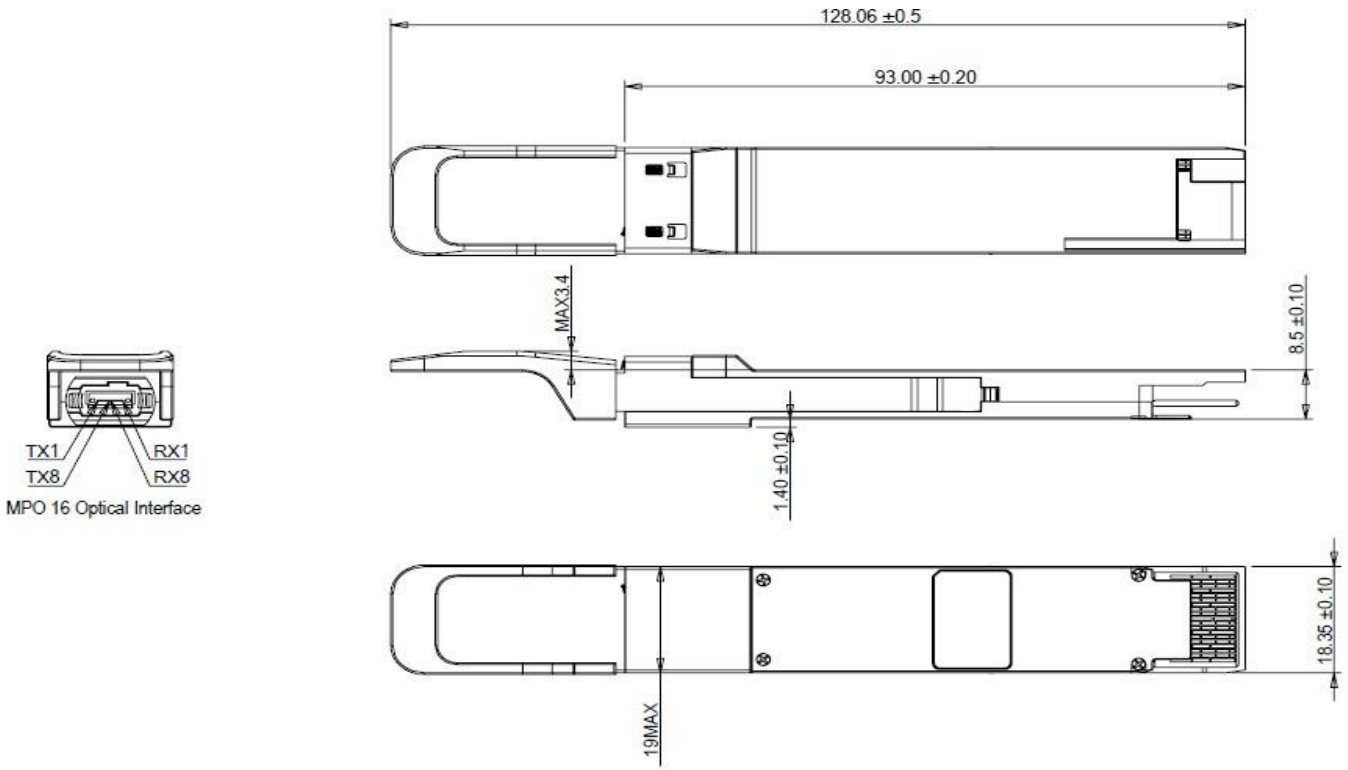
Pin Description

| Pin# | Logic | Symbol | Description | Plug Sequence |
|------|-------------|---------|-------------------------------------|---------------|
| 1 | | GND | Ground | 1B |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3B |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3B |
| 4 | | GND | Ground | 1B |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3B |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3B |
| 7 | | GND | Ground | 1B |
| 8 | LVTTL-I | ModSelL | Module Select | 3B |
| 9 | LVTTL-I | ResetL | Module Reset | 3B |
| 10 | | VccRx | +3.3V Power Supply Receiver | 2B |
| 11 | LVC MOS-I/O | SCL | 2-wire serial interface clock | 3B |
| 12 | LVC MOS-I/O | SDA | 2-wire serial interface data | 3B |
| 13 | | GND | Ground | 1B |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3B |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3B |
| 16 | GND | Ground | 1B | |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3B |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3B |
| 19 | | GND | Ground | 1B |

| Pin# | Logic | Symbol | Description | Plug Sequence |
|------|---------|----------|---|---------------|
| 20 | | GND | Ground | 1B |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3B |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3B |
| 23 | | GND | Ground | 1B |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3B |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3B |
| 26 | | GND | Ground | 1B |
| 27 | LVTTL-O | ModPrsL | Module Present | 3B |
| 28 | LVTTL-O | IntL | Interrupt | 3B |
| 29 | | VccTx | +3.3V Power supply transmitter | 2B |
| 30 | | Vcc1 | +3.3V Power supply | 2B |
| 31 | LVTTL-I | InitMode | Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE | 3B |
| 32 | | GND | Ground | 1B |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3B |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3B |
| 35 | | GND | Ground | 1B |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3B |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3B |
| 38 | | GND | Ground | 1B |
| 39 | | GND | Ground | 1A |
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input | 3A |
| 41 | CML-I | Tx6p | Transmitter Non-Inverted Data Input | 3A |
| 42 | | GND | Ground | 1A |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input | 3A |
| 44 | CML-I | Tx8p | Transmitter Non-Inverted Data Input | 3A |
| 45 | | GND | Ground | 1A |
| 46 | | Reserved | For future use | 3A |
| 47 | | VS1 | Module Vendor Specific 1 | 3A |
| 48 | | VccRx1 | 3.3V Power Supply | 2A |
| 49 | | VS2 | Module Vendor Specific 2 | 3A |
| 50 | | VS3 | Module Vendor Specific 3 | 3A |
| 51 | | GND | Ground | 1A |
| 52 | CML-O | Rx7p | Receiver Non-Inverted Data Output | 3A |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output | 3A |
| 54 | | GND | Ground | 1A |
| 55 | CML-O | Rx5p | Receiver Non-Inverted Data Output | 3A |

| Pin# | Logic | Symbol | Description | Plug Sequence |
|------|-------|----------|-------------------------------------|---------------|
| 56 | CML-O | Rx5n | Receiver Inverted Data Output | 3A |
| 57 | | GND | Ground | 1A |
| 58 | | GND | Ground | 1A |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output | 3A |
| 60 | CML-O | Rx6p | Receiver Non-Inverted Data Output | 3A |
| 61 | | GND | Ground | 1A |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output | 3A |
| 63 | CML-O | Rx8p | Receiver Non-Inverted Data Output | 3A |
| 64 | | GND | Ground | 1A |
| 65 | | NC | No Connect | 3A |
| 66 | | Reserved | For future use | 3A |
| 67 | | VccTx1 | 3.3V Power Supply | 2A |
| 68 | | Vcc2 | 3.3V Power Supply | 2A |
| 69 | | Reserved | For Future Use | 3A |
| 70 | | GND | Ground | 1A |
| 71 | CML-I | Tx7p | Transmitter Non-Inverted Data Input | 3A |
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input | 3A |
| 73 | | GND | Ground | 1A |
| 74 | CML-I | Tx5p | Transmitter Non-Inverted Data Input | 3A |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input | 3A |
| 76 | | GND | Ground | 1A |

Dimensions



QSFP- DD SR8 MPO 16 Optical Interface Outline



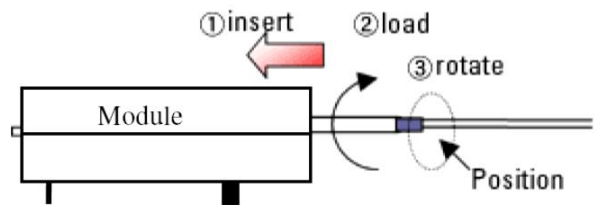
Optical Receptacle Cleaning Recommendations:

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.

Cleaning of patch-cord



Cleaning of fiber stub

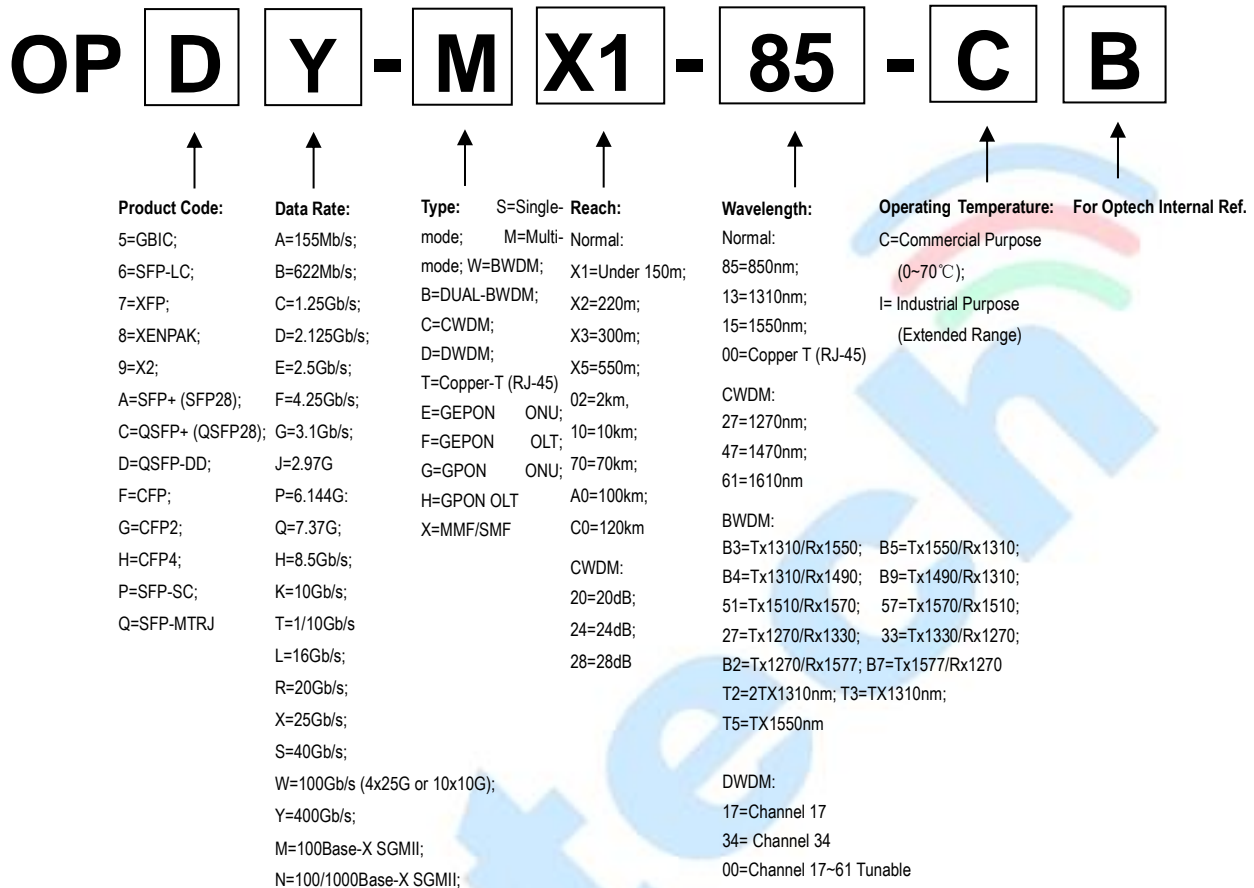


1. Insert
Ensure that stick is held straight when inserting into sleeve.
2. Load
Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve.
3. Rotate
Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained.

*Notice: Number of possible wipes:
Maintenance (repair) ~1 use / piece
Equipment construction: 4 uses / piece (max.)*

Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information



| Model Number | Part Number | Voltage | Temperature |
|------------------|----------------|---------|--------------|
| QSFP-DD-400G-SR8 | OPDY-MX1-85-CB | 3.3V | 20°C to 60°C |

Note: All information contained in this document is subject to change without notice.